ANALOG-TO-DIGITAL SYSTEM

by

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Research Report Number 73-4

Development of a System for High-Speed
Measurement of Pavement Roughness

Research Project 3-8-63-73

conducted for

The Texas Highway Department

in cooperation with the
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The opinions, findings, and conclusions expressed in this publication are those of the authors and not necessarily those of the Bureau of Public Roads.

PREFACE

This is the fourth in a series of reports presenting results from Research Project No. 3-8-63-73, "Development of a System for High-Speed Measurement of Pavement Roughness." The project was initiated in 1963 for the purpose of evaluating the existing roughness measuring devices and providing to the sponsors a recommendation as to the best existing system for accurate measurement of road profiles. In the first report, 73-1, "High-Speed Road Profile Equipment Evaluation," the General Motors Road Profilometer was recommended and after authorization from the Bureau of Public Roads a contract was initiated with the company licensed to manufacture it.

The profilometer, called the Surface Dynamics (SD) Profilometer, was manufactured by K. J. Law Engineers, Inc., and was delivered to the Texas Highway Department on February 6, 1967. This report describes the analog-to-digital process used in the measuring system.

This project is sponsored by the Texas Highway Department and the U. S. Department of Transportation Bureau of Public Roads. The special assistance of Texas Highway Department Representative Kenneth Hankins is appreciated, as is the help of Messrs. Larry G. Walker, Wilbert Hall, Bob Choate, and Tom Hill of the Texas Highway Department Division of Automation.

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LIST OF REPORTS

Report No. 73-1, "High-Speed Road Profile Equipment Evaluation," by W. Ronald Hudson, presents a review of existing roughness measuring equipment and recommends the GM Profilometer as the most promising of all available equipment for high-speed profile measurements.

Report No. 73-2, "A Profile Measuring, Recording, and Processing System," by Roger S. Walker, Freddy L. Roberts, and W. Ronald Hudson, presents a description of the Surface Dynamics Profilometer profile measuring system, an operating procedure for use with the equipment, and a system analysis procedure for validation of the profile data.

Report No. 73-3, "Pavement Serviceability Equations Using the Surface Dynamics Profilometer," by Freddy L. Roberts and W. Ronald Hudson, presents a brief description of the measuring system, a complete description and analysis of three rating sessions, and the development of equations relating the mean panel rating to various summary statistics. Equations for predicting PSI for both flexible and rigid pavements are presented.

Report No. 73-4, "Analog-to-Digital System," by Roger S. Walker, and W. Ronald Hudson, describes the Hewlett-Packard 2115 computer analog-to-digital computing facility.

ABSTRACT

The Hewlett-Packard 2115 analog-to-digital (A-D) facility purchased for data processing in conjunction with the SD Profilometer is described in this report. Included is a general discussion of the A-D problem and the various subsystems in the A-D system. A detailed description is provided for: (1) an interface and patch logic module which was built by project personnel to interface external signs with this facility; (2) the A-D and Tape Write programs necessary for system operations; and (3) the operating and data validation procedures required to use the equipment. All additional interface cabling and hardware diagrams and computer program listings that are necessary for complete documentation of the A-D system are also included.

KEY WORDS: SD Profilometer, HP 2115 computer, analog-to-digital converter (multiverter), pulse generator, interface and patch logic module, Honeywell FM analog recorder.

SUMMARY

The system described in this report provides the Texas Highway Department with an extremely powerful high-speed Analog-to-Digital facility for use with Project 73 as well as other highway research department projects.

Earlier research in this project had used rented equipment for A-D operation (Ref 2), but because of difficulties in using the system and the need for permanent operations it was decided to purchase a stand-alone system.

Upon considering the rather general A-D requirements for Project 73, it was decided to also include the additions necessary for providing a general purpose capability in the A-D system to be purchased as it was found that such capability could be obtained at very little additional cost. A Hewlett Packard 2115 computer system was purchased for providing this capability and is described in this report.

The A-D system was also designed to maintain complete compatability with the SDS 930 system. That is, a digital tape containing digitized profile data obtained from the SDS 930 system is in the same format as one run on the HP system and current analysis programs that run on either the CDC 6600 or IBM 360/50 systems can use these data without program changes.

IMPLEMENTATION STATEMENT

The A-D system described in this report was developed primarily for its use in digitizing road profile data obtained from the SD Profilometer. Because of the need for an analog-to-digital facility for other research projects at the Texas Highway Department, a general-purpose A-D capability was incorporated in the systems design. This general-purpose capability can be noted by its use in Project 3-8-67-108 on weighing in motion. The modular systems design characteristic of the IPLM and system programs permits flexibility in adding any additional requirements which might be needed by these or other research projects.

In summary, the system described herein provides the Texas Highway Department with an extremely powerful high-speed general-purpose A-D facility.

TABLE OF CONTENTS

NOMENCLATURE

va	=	volt-amps
hz	=	Hertz
vac	=	volts alternating current
vdc	=	volts direct current
Khz	=	kilohertz
db	=	decibels
FM	=	frequency modulation
bpi	=	bits per inch
ma	=	milliamperes
μ sec	=	microseconds
η sec	=	nanoseconds
LSB	=	least significant bit

CHAPTER 1. INTRODUCTION

This report supplements Research Report No. 73-2, entitled "A Profile Measuring, Recording, and Processing System," by providing a description of Hewlett-Packard 2115 analog-to-digital (A-D) computing system. Research Report No. 73-2 describes the SDS 930 system which was rented for use during the earlier part of Project 3-8-63-73 for A-D operations. However, because of difficulties in using this system and the need for permanent operations it was decided to purchase a stand-alone system for this and other research projects at the Texas Highway Department (THD). The Hewlett-Packard system described herein was selected for this stand-alone facility.

Background

Interest in purchasing a high-speed A-D facility for Project 73 existed at the beginning of the project, and considerable time was spent by project personnel in investigations of existing and available equipment. It was decided, however, to wait until project requirements were better defined before purchasing such a system. The University soon installed an SDS 930 computer system which had an A-D peripheral unit, and this system was integrated into Project 73 to provide the necessary A-D requirements. It is discussed in Research Report No. 73-2. During the fall of 1967, difficulties in using this system once again prompted interest in purchasing a stand-alone system. After discussions with the THD, project personnel again began reviewing existing systems. During the spring of 1968, a request for proposals which specified the A-D requirements was prepared and provided to the THD by project personnel. After all bids were reviewed, a Hewlett-Packard 2115 computer system was selected. The system was delivered in February 1969.

Use by Other Projects

Because of the rather general A-D requirements for Project 73, it was

decided to include the additions necessary for providing a general-purpose facility in the A-D system to be purchased. It was found that such capability could be obtained at very little additional cost. Thus, the HP system purchased and described in this report includes this additional capability.

The A-D system was also designed to maintain complete compatability with the SDS 930 system. That is, a digital tape containing digitized profile data obtained from the SDS 930 system is in the same format as one run on the HP system and current analysis programs that run on either the CDC 6600 or IBM 360/50 systems can use these data without program changes.

CHAPTER 2. SYSTEM DESCRIPTION

The analog-to-digital system is used to convert analog signals (such as the analog profile signals obtained by the profilometer) into discrete or digital values for digital computer analysis. This chapter describes the Hewlett-Packard (HP) 2115 A-D system and provides a description of the functions and interface requirements of each major subsystem. Subsequent chapters provide the hardware and software details on the individual units.

The HP 2115 A-D system purchased from the Hewlett-Packard Company is illustrated in Fig 2.1. Figure 2.2 expresses symbolically the HP system. As noted in Fig 2.2, the system consists of a 2115A Central Processing Unit, 8,192 words of core memory, two direct memory access channels, a Raytheon Multiverter, a high-speed tape reader, an ASR 35 teletypewriter, a positive logic duplex register for special purpose interface, and two tape units (a nine-track high-speed unit and a seven-track low-speed unit).

For A-D operations, an interface unit was required (see IPLM description below) to interface the external begin conversion commands necessary for the A-D operation requirements. This unit is connected to the positive duplex register.

Analog-to-Digital Process

Basically, all current research projects requiring A-D operations involve (1) recording the analog data at the test site; (2) bringing these data back to the laboratory for examination and validation; (3) if acceptable, digitizing the analog data; and (4) running the digital analysis programs on these data at the central computing facility (CDC 6600 or IBM 360/50). Figure 2.3 illustrates this general data collection procedure. As described in Research Report No. 73-2, this is the procedure used for obtaining road profile data.

The A-D system is expressed symbolically in Fig 2.4. As indicated in this figure, the system receives inputs from the analog data channels and A-D command information. Two A-D programs are used by the system for first

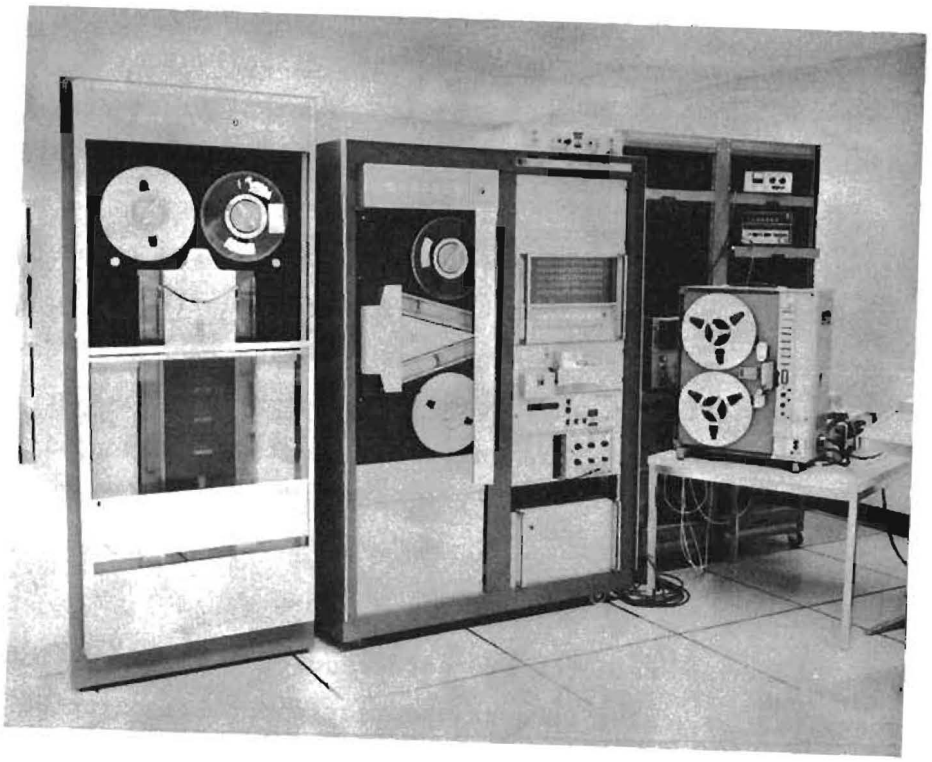

Fig 2.1. Hewlett-Packard 2115 analog-to-digital system.

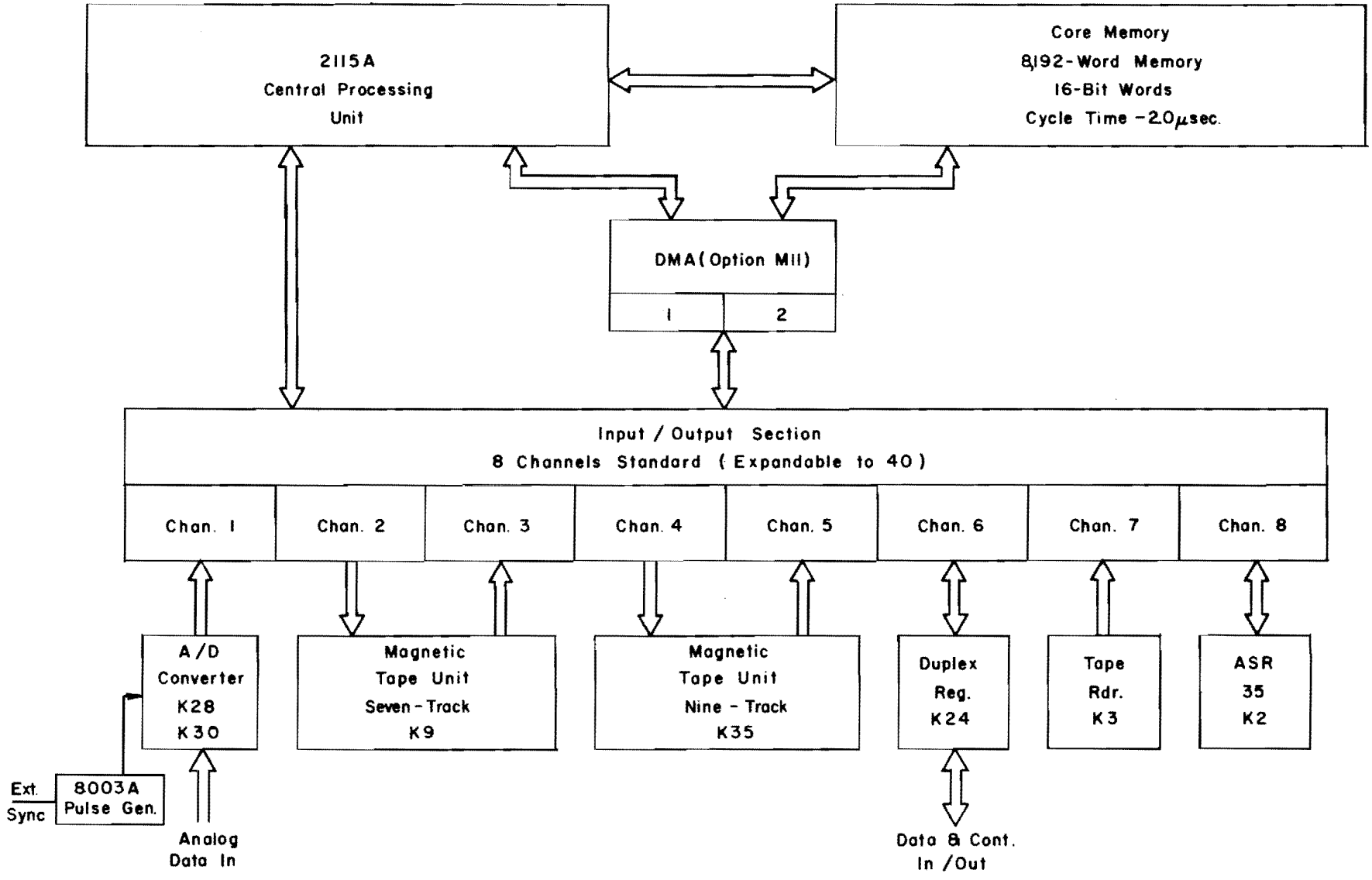

Fig 2.2. HP A-D computing facility.

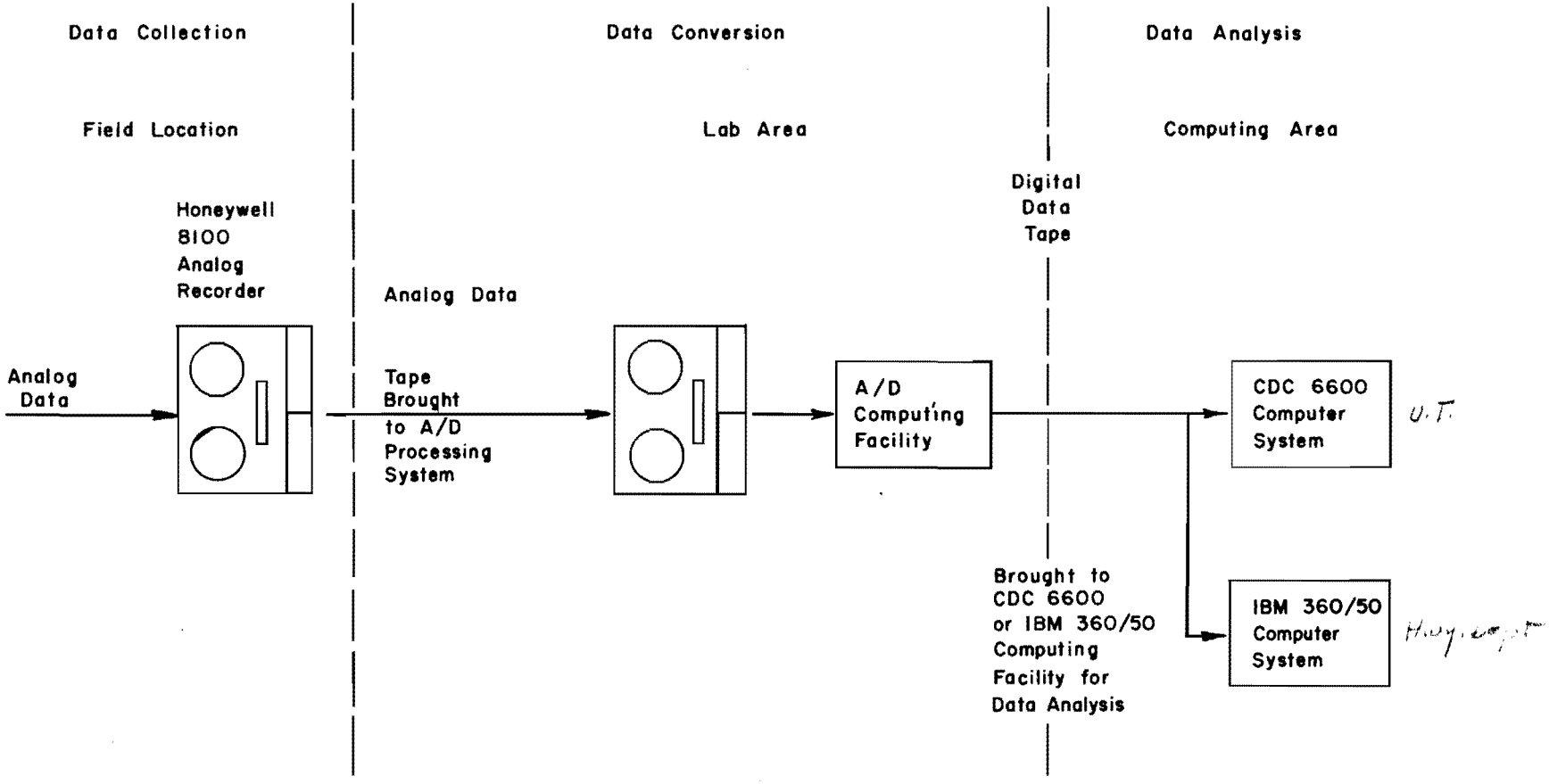

Fig 2.3. A-D data collection.

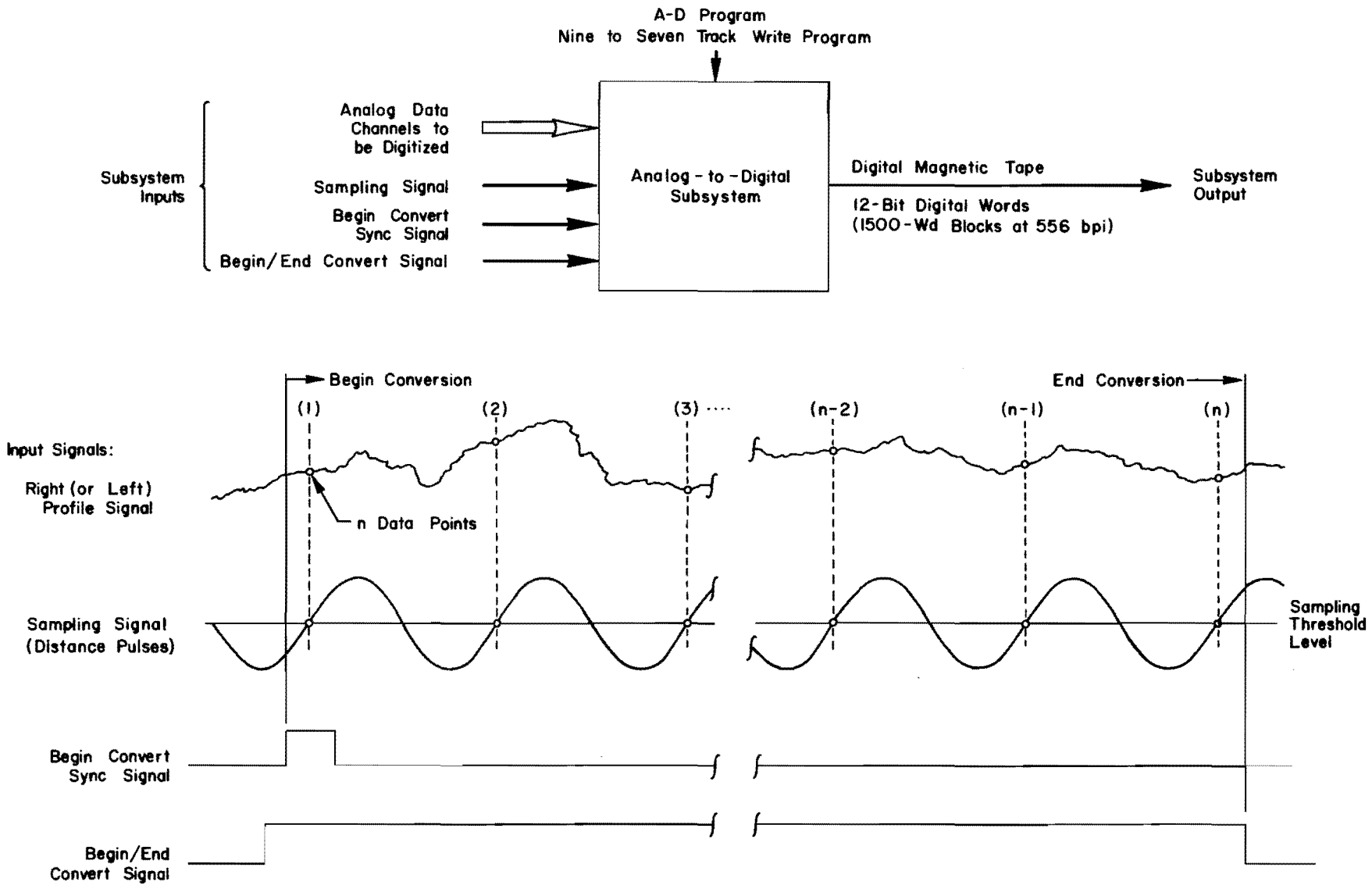

Fig 2.4. Analog-to-digital subsystem.

digitizing the data and writing it on the nine-track tape, and then transferring the data to a seven-track tape in a format compatible with the SDS system. The system provides, as an output, the digitized data tape which may then be used by data analysis programs on either the CDC 6600 or IBM 360/50 systems.

Of the eleven input signals depicted in Fig 2.4, eight of them provide the system with the analog data to be digitized. The remaining three command signals provide the external sampling signal, the begin/end convert signal, and the begin convert synchronizing (sync) signal*. The begin/end convert signal comes up first, initializing the system. The program then waits until the begin convert sync signal comes up, which indicates the beginning of the digitization process. For profile data (see Research Report 73-2), the begin convert sync signal input is driven by the photocell signal, and when sensed by the computer, indicates the beginning of the section to be measured and hence the beginning of the conversion process. Once the conversion process has begun, it continues in accordance with the sampling signal (distance pulses from the profilometer) until the begin/end convert signal drops. This indicates the end of the conversion process and thus the end of the digitized data file. The begin/end convert signal is initiated and terminated manually. For the profilometer data, this signal is controlled by the operator from commands given by the profilometer operator via the Honeywell recorder voice channel. A switch on the IPLM (see IPLM description, Chapter 3) overrides the begin convert sync signal so that the process can be completely controlled by the manual begin/end convert signal. The IPLM and A-D program may be modified so that the conversion process can be controlled entirely by a synchronized convert signal or any other desired external signal combinations.

Once the conversion process begins, the analog data are digitized and stored into 1500-word blocks and then written on a nine-track digital magnetic tape at 800 bpi. Two memory buffers are used by the computer, one for inputting the digitized values, and the other for outputting the data on the digital tape. Upon receipt of the end of convert signal, a five-word

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* The begin convert sync signal can easily be modified (see interface and patch logic module description, Chapter 3) to provide both a begin/end or end only synchronized signal.

identification record followed by an end of file is written, signifying the end of the conversion process and the data file.

After the data have been digitized and written on the nine-track high-speed tape unit, a second program is then used for transferring these data to the seven-track unit in a form compatible with the SDS 930 system (see Research Report No. 73-2).

Figure 2.5 illustrates the A-D system interface configuration. Six subsystems are depicted in this figure: (1) the Honeywell 8100 recorder, (2) the interface and patch logic module (IPLM), (3) the HP pulse generator, (4) the Raytheon A/D multiverter, and (5) the HP 2115 computer system. In this figure, data and command information are transferred from the Honeywell 8100 analog recorder to the IPLM. The IPLM is used to patch the proper data and command signals for the digitization process. It also contains the necessary signals for interfacing these data and command information to the 2115 computer and Raytheon multiverter. Command information is sent to the positive logic duplex register which interfaces these data with the 2115 data channel as depicted. The external sampling signal for synchronized sampling control is transferred to the HP pulse generator where it is shaped and gated (by program control) into the Raytheon unit.

Analog Recorder

Data are recorded at the test site on a Honeywell eight-channel (plus one voice channel) recorder. After validation of these data it is played back into the IPLM by the same or a similar recorder at the A-D computer facility. The calibrated output range of the recorder is ± 2 volts peak-to-peak. Since the Raytheon multiverter input range is ± 5 volts peak-to-peak, for a 2-volt recorder signal, resolution is reduced to two-fifths of its full-scale value. Thus a digital value of 820 would represent a positive 2-volt tape recorder signal as opposed to 2,048 for a 5-volt full-scale value. An edge-track voice channel is also included along with the eight analog data channels and can be used for recording voice or other low-fidelity A.C. signals. Table 2.1 provides the Honeywell 8100 FM tape recorder specifications.

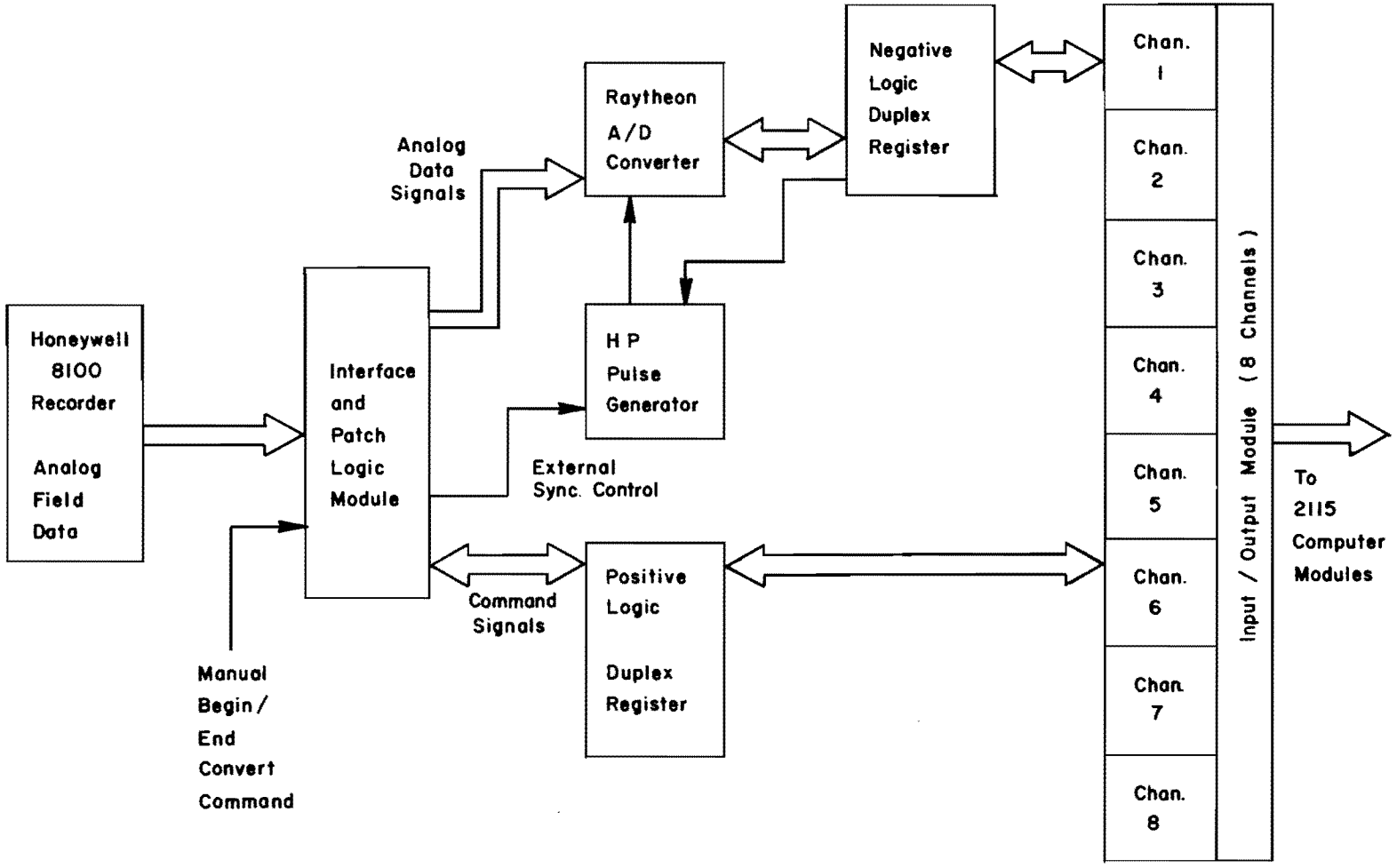

Fig 2.5. Analog-to-digital system interface configuration.

TABLE 2.1. HONEYWELL 8100 RECORDER SPECIFICATIONS

REEL SIZE: 10 1/2" maximum NAB Hub
TAPE SPEEDS: 30, 15, 3 3/4, 1 7/8
BRAKING: Dynamic for all modes, mechanical holding brakes
MOTOR POWER: DC for supply, take up and capstan
SPEED CONTROL: Electronic phase comparison from tone wheel
SPEED CHANGE: Front panel electrical switching
REWIND TIME (1 MIL BASE): 4 minutes maximum
SPEED ACCURACY: Within 0.5% of nominal

FM Data Channels:

Extended Mode (Std. all models)

Tape Speed (IPS)	CF (KC)	Data Bandwidth (KC)
30	54	0-10
15	27	0-5
3 3/4	6.75	0-1.25
1 7/8	3.375	0-0.625

IRIG Std. Mode (available by switch, 8107 only)

Tape Speed (IPS)	CF (KC)	Data Bandwidth (KC)
30	27	0-5
3 3/4	3.375	0-0.625

INPUT SENSITIVITY: ±2v peak minimum to ±10v peak maximum (for ± 40% deviation)
INPUT IMPEDANCE: 10K ohms, single ended
OUTPUT LEVEL: ± 2v peak at ± 5Ma maximum undistorted output for ± 40% deviation
OUTPUT IMPEDANCE: Less than 50 Ohms
HARMONIC DISTORTION: Less than 2% total 2nd and 3rd throughout passband
FREQUENCY RESPONSE: ±0.25db DC to 0.5 full bandwidth, maximum 1 db down at cutoff
LINEARITY: Less than 2% of full scale (± 40%) deviation from best straight line through zero center.
DRIFT:
Center Frequency: Less than 2% of full scale (± 40%) typical over operating temperature range
Sensitivity: Less than 2% of full scale (± 40%) typical over operating temperature range (less than 1% change in center frequency or sensitivity over 24 hrs. in a 10° F temperature range)

CONTROLS:
Oscillator: Center frequency and input sensitivity
Discriminator: Zero adjust and output level
CENTER FREQUENCY SELECTION:
Oscillator: Four incorporated, selected by transport speed control switch
Discriminator: Maximum two speeds plug-in simultaneously. Selection between the two by transport speed control switch.

SIGNAL TO NOISE RATIO:
(Defined as the ratio of a full scale sine wave output to the residual noise present with oscillator input shorted.)

Tape Speed	Bandwidth	S/N Ratio (db)	
		comp.	uncomp.
30	0-10 KC	45	42
15	0-5 KC	45	42
3 3/4	0-1.25 KC	42	36
1 7/8	0-0.625 KC	42	36

D. Calibration Unit:

Integral on all models
FUNCTIONS: Set oscillator and discriminator center frequency and deviation
FREQUENCY SOURCE: Crystal oscillators
ADJUSTMENT ACCURACY: ± 1%—deviation and center frequency
CONTROLS: Meter sensitivity, channel selector, function selector

Interface and Patch Logic Module (IPLM)

The interface and patch logic module (IPLM) was built by project personnel to interface the analog data and command signals with the HP 2115 system. The three main functions of the IPLM are:

(1) to provide a patching network for connecting the analog data and command signals to the proper data and command signals of the A-D system,

(2) to boost and shape the command information signals from the Honeywell recorder voltage levels to the proper voltage levels for interface with the HP duplex register, and

(3) to generate the proper command signals (flag) for communication with the HP duplex register.

A complete hardware description of the IPLM is provided in Chapter 3. Briefly, however, the IPLM receives inputs from the Honeywell recorder and the manual begin/end convert command. The eight analog input and one voice channels may be patched to any A-D input channel or command channel via the patching cables on the IPLM. The manual begin/end convert signal and the begin convert sync signal are switched directly to line 0 and line 1, respectively, of the positive logic duplex register. The IPLM also interfaces the external sampling signal to the HP pulse generator. The IPLM generates a flag signal for signaling when data are to be read by the positive logic duplex register. Table 2.2 provides the hardware specification for the IPLM.

TABLE 2.2. IPLM SPECIFICATIONS

Power requirement - 110 volts A.C.

Size - 17 x 12 x 3 inches

INPUTS

Front

Begin/end convert switch - single pole double throw

Rear

Eight analog channels - 16-pin Blue Ribbon connector

Voice channel - BNC connector

Begin/end convert sync - BNC connector

OUTPUTS

Rear

Eight analog channels - 16-pin Blue Ribbon connector

Sixteen channel duplex - 32-pin Blue Ribbon connector

Voice channel - BNC connector

Flag signal - BNC connector

Note: Analog channel inputs may be patched to analog channel outputs in any desired combination.

Begin/End Convert Sync Input Requirement

Positive mode - sensitivity: requires minimum 2-volt positive going input (not to exceed 12 volts)

Input Impedance

12k ohms

Flag Output

Output level - 0 to 12 volts

Note: 10 to 12 volts corresponds to logic 0; 0 to 2.5 volts corresponds to logic 1.

(Continued)

TABLE 2.2. (CONTINUED)

Flag goes from 0 to 1 for three conditions:

(1) begin/end convert switch turned on,

(2) begin/end convert switch turned off, and

(3) begin/end convert sync signal turned on.

Output impedance - 1k ohms

Length of flag signal - 40 μ sec

Rise time - 8 μ sec

Fall time - 400 n sec

Duplex Outputs

Output levels - 0 to 2.5 volts → logical 1

5.5 to 10.5 volts → logical 0

Output impedance - 800 ohms

FEATURES

(1) Begin/end convert sync signal can be either a positive going or negative going signal.

(2) Duplex line 1 (2nd line) can be held at logical 1 if the begin/end convert sync is not going to be used. (This corresponds to the "Inhibit" position on interface.)

(3) Indicating circuit with light can be used to determine when flag signal is sent.

(4) Test mode which enables quick checkout of duplex lines 0 and 1 by using begin/end convert switch to input signals.

(5) Patch board provides any desired combinations of input analog channels to output analog channels.

INTERNAL POWER SUPPLY

± 10 volts D.C. with less than 2 percent ripple.

HP 8003 Pulse Generator and Raytheon Multiverter

A Hewlett-Packard 8003A pulse generator is used in the system for interfacing the sampling signal from the IPLM or from an external source to the Raytheon multiverter. The pulse generator has three primary purposes:

(1) It provides the proper pulse characteristics, i.e., pulse width, height, and rise and fall time.

(2) It permits the gating of pulses by program control thus providing proper synchronization for external triggering.

(3) It provides an internal source for a wide range of selectable sampling rates.

The trigger input connector on the pulse generator is used for the external sampling signal. It is gated* accordingly to program control (if gating is selected), shaped, and sent out to the multiverter via the negative trigger output terminal.

Pulse amplitude, width, and frequency may be varied by the manual adjustments located on the front of the unit. See Table 2.3 for specifications on the HP 8003A pulse generator.

A Raytheon multiverter model RC 3013 is used in the system for digitizing the analog data. Although the unit was built by Raytheon, it is a standard item for HP systems and thus supported by HP field personnel. The multiverter has been modified by HP to interface directly with the HP negative logic duplex register and to provide full-scale resolution for 5-volt analog input signals. The multiverter is capable of handling up to 8 analog input channels for digitization.

The multiverter consists of three subunits: a multiplexer unit, a sample-and-hold amplifier, and an analog-to-digital converter. The sample-and-hold unit samples the analog channel as directed by the multiplexer logic and holds the data until they are digitized by the A-D unit. Because there is only one sample-and-hold unit, the sampling time difference between successive channels is dependent on the sampling rate.

Four modes of A-D sampling are possible, including a calibrate mode. The other three modes (random address, digitize-only, and sequence) differ

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* A gate switch at the rear of the multiverter is used for selecting gated or free running pulse control.

TABLE 2.3. 8003A PULSE GENERATOR SPECIFICATIONS

OUTPUT PULSE

SOURCE IMPEDANCE: 50Ω ±3% shunted by typically 20 pF at any output voltage.

PULSE SHAPE: (Measured at 5 V across 50Ω)
- Rise and Fall time: Less than 5 ns
- Overshoot and Ringing: Less than 5% of pulse amplitude.
- Preshoot: Less than 5% of pulse amplitude.

AMPLITUDE: (Positive and negative output can be independently set)
- Maximum Output: 5V across 50Ω (10V across an open circuit). Output circuit protected, cannot be damaged by shorting. With internal load disconnected (switch provided), 10V across 50Ω with rise and fall time less than 7 ns.
- Attenuator: Provides 7 steps from 0.05V to 5V in a 1, 2.5, 5 sequence.
- Vernier: Provides continuous adjustment between ranges, minimum output less than 0.02V across 50Ω.

POLARITY: Positive and negative simultaneously. Delay between pulses approximately 5 ns.

PULSE WIDTH: 30 ns to 3 s in five ranges; vernier provides continuous adjustment between ranges.
- Maximum Duty Cycle:
  - Greater than 90% from 0.3Hz to 1MHz
  - Greater than 50% from 1MHz to 10MHz
- Width Jitter: Less than 0.1% of pulse width at any width setting.

DELAY: Approximately 150ns fixed delay between Trigger Output and both Pulse Outputs. Internal slide switch permits removal of delay line, reducing delay to about 10 ns.

REPETITION RATE AND TRIGGER

FREE-RUNNING:
- Repetition Rate: 0.3Hz to 10MHz in five ranges; vernier provides continuous adjustment between ranges.
- Period Jitter: < 0.1% of period at any repetition rate setting.

TRIGGERING:
- Trigger Input: DC coupled. Sine waves or pulses of either positive or negative polarity up to 10MHz.
- Sensitivity: Sine waves, 2V pk-pk minimum. External Pulses, at least 1V and at least 15ns wide, Maximum input ±10V.
- External Trigger Delay: Approximately 35 ns between trigger input and trigger output.
- Manual: Push button for single pulse.

TRIGGER OUTPUT PULSE (Suitable for triggering another Model 8003A).
- Width: 15ns ±5ns at 50% amplitude points.
- Amplitude: Greater than 2V across 50Ω.
- Polarity: Positive.

SYNCHRONOUS GATING: Gating signal turns generator "on"; pulse repetition rate, amplitude, polarity, and width determined by panel control settings; first pulse is coincident with the leading edge of the gate, last pulse is completed even if gate ends during the pulse.

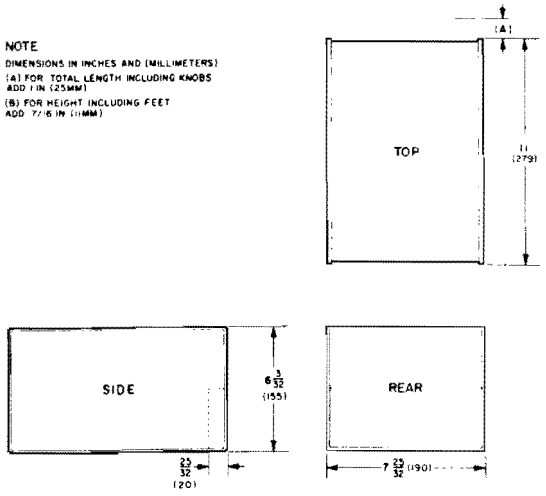
- Minimum Gating Signal: -2V.
- Maximum Input: -20V.
- Input Impedance: Approximately 1kΩ.

GENERAL

POWER 115V or 230V +10% -15%, 50Hz - 400Hz, 30W.

WEIGHT: Net 9 lb (4 kg)
Shipping 13 lb (6 kg).

DIMENSIONS:



in the selection technique of the analog channels to be digitized. The random-address mode allows individual selection of the analog channels by program control thus permitting random channel selection. The digitize-only mode permits continuous digitization of the same analog input channel by a single initiating channel address instruction. The sequence mode, which is used by the current A-D program, permits automatic sampling of each channel sequentially, cycling back to the first channel at the completion of the sequence. For the sequence mode the octal channel number of the last channel to be converted is entered into the multiplexer logic through the octal channel select switches on the front of the multiverter.

The external sampling command signal controls the rate of sampling. For the current system this signal comes from the pulse generator. Hence, it may be triggered by some external signal, such as a signal on one of the Honeywell analog recorder channels or from its own internally generated signal (see pulse generator specifications).

The sampling signal characteristics are important and should be noted in the multiverter specifications (Table 2.4).

IPLM Interface, Positive Logic Duplex Register

A positive logic duplex register was included by HP to meet the requirements of providing the external communication capability for such signals as the begin/end convert signal, the begin convert synchronizing signal, etc. This register provides 16 input and 16 output lines, a flag signal, and an encode command signal. Currently, only lines 0 and 1 of the duplex input are used. Line 0 is used for the begin/end convert signal and line 1 is used for the begin convert sychronizing signal. When activated, line 1 will control the begin conversion process. The command signal will not be used by the control lines but should be set by the STC or encode command. Data transfer will then be handled by the flag signal which will be set each time an external command is initiated.

System Capabilities

The A-D system has the following capabilities:

(1) Samples up to 8 analog data channels at rates to 24 Khz. The Raytheon multiverter multiplexes each of the 8 input channels

TABLE 2.4. STANDARD MULTIVERTER CHARACTERISTICS

	2's Complement Sign	
+ Full scale (-1 count)	0	1111111111
+ 1/2 Full scale	0	1000000000
Zero (+1 count)	0	0000000001
Zero	0	0000000000
Zero (-1 count)	1	1111111111
- 1/2 Full scale	1	1000000000
- Full scale (-1 count)	1	0000000001

Clock Output . . . . . Transformer-coupled 8-volt pulse of 0.2-usec duration (isolated secondary)
Z_o=10 ohms
I_{max}=20 ma

Serial Output . . . . . Same as clock output. A pulse is produced every time a binary zero is generated during the conversion.

MODES OF OPERATION

Random Address . . . . . Externally controlled
Sequence . . . . . Externally controlled
Digitize Only . . . . . Externally controlled
Calibrate . . . . . Manually controlled

TEMPERATURE

Temperature Range . . . . . 0 to 50°C
(For extended ranges see Note 3.)
Warmup Time . . . . . 10 min to rated accuracy
Cooling . . . . . Forced air
Temperature Coefficient . . . . . 10 ppm/°C(max)

MECHANICAL

Analog Input Connectors . . . . . Malco connector panel or optional coax panel
Digital Input Connector (mating) . . . . . Amphenol Type 17-20500-1 or Cannon Type DD-50P
Register Display . . . . . Amperex indicators
Size . . . . . 19" slide-mounted drawer, 22" deep x 5-1/4" high
Weight . . . . . 60 pounds (approx)
Power . . . . . 105 to 125 vac 60 to 400 cps (fused at 3 amp, slow blow)

ANALOG INPUT

Channel Capacity . . . . . 96 Channels w/o attenuators
48 channels w/attenuators
Crosstalk . . . . . 80 db with 1K source at 400 cps (See Note 1.)
Aperture Time . . . . . 50 nanoseconds (See Note 2.)
Input Voltage Range . . . . . ±10 volts full scale w/o attenuators
±100 volts full scale w/attenuators

Input Impedance
(w/o attenuators) . . . . . 100 meg min for selected channel
1000 meg min for unselected channel
(w/attenuators) . . . . . 20K (±0.02%) for either selected or unselected channels
Max Source Impedance . . . . . 1000 ohms for specified performance w/o attenuators
Max Voltage Overload . . . . . 100% of full scale w/o attenuators
125% of full scale w/attenuators

PERFORMANCE

Accuracy at DC
Linearity . . . . . 0.01% ±1/2 LSB
Long Term Drift . . . . . 0.01% (typical)
Temp Coefficient . . . . . 10 ppm/°C (max)
Voltage Ref Stability 0.001%
Typical accuracy at 25°C will be within 0.02% of full scale ±1/2 LSB

DIGITAL INPUTS

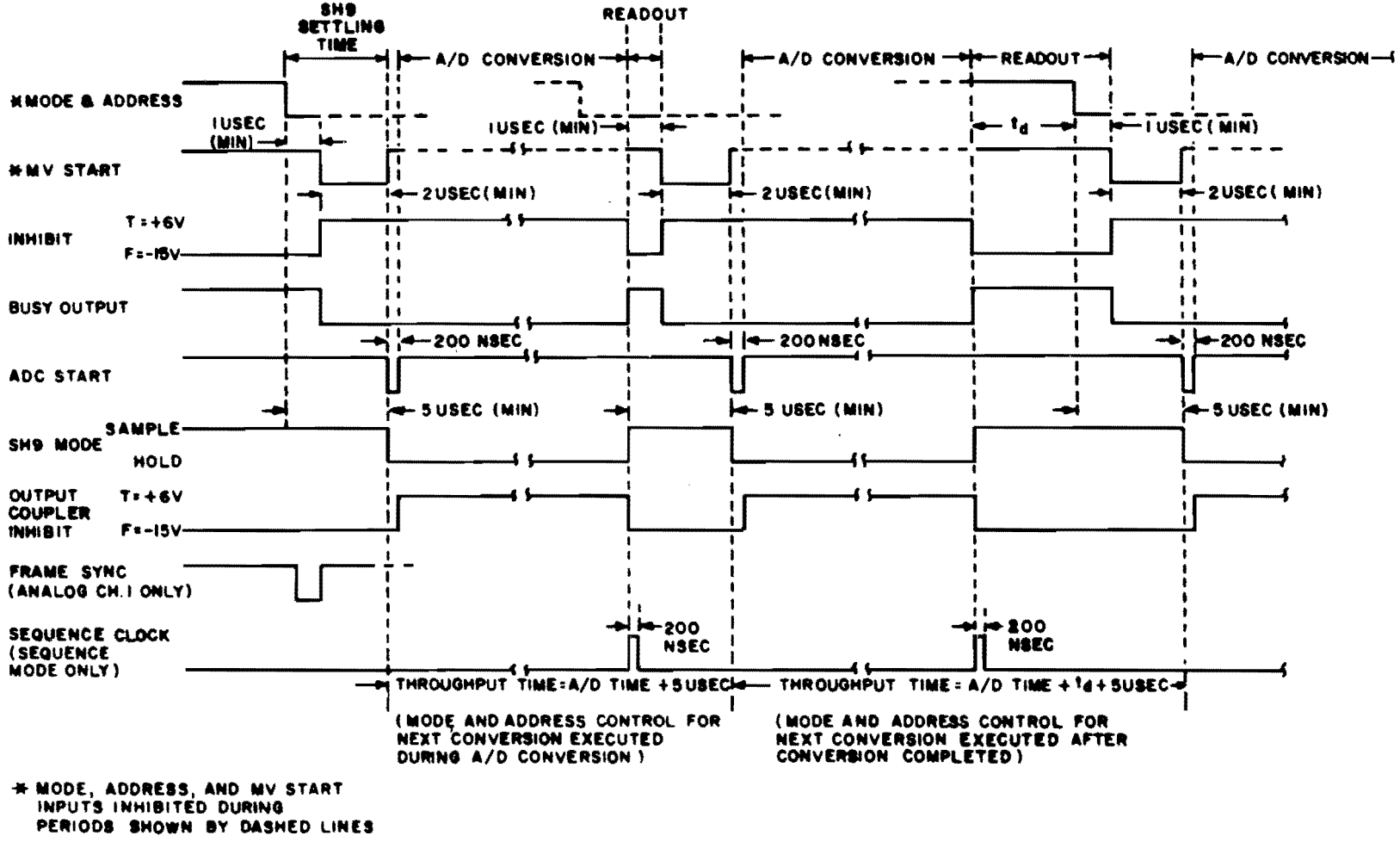
Logic Level (input) . . . . . Binary 1=-6 to -12 volts
Binary 0=0 ±1 volt
Start Line (1 line) . . . . . Z_{in}=3K to -15 volts
Channel Address (7 lines max) . . . . Z_{in}=1.8K to -15 volts
Mode Selection (2 lines) . . . . . Z_{in}=3.9K to -15 volts

DIGITAL OUTPUTS

Parallel Data Outputs . . . . . Refer to attached ADC manual
Multiverter "Busy" . . . . . Refer to attached ADC manual
Frame Sync . . . . . 3.9K to -15 volts

(Continued)

TABLE 2.4. (Continued)



* MODE, ADDRESS, AND MV START INPUTS INHIBITED DURING PERIODS SHOWN BY DASHED LINES

through a single sample and hold circuit. Thus, individual channel sampling rates are governed by Eq 2.1:

$$R = \frac{23}{N} \tag{2.1}$$

where

R = sampling rate in Khz per channel,

N = number of channels used.

The 23 Khz maximum sampling rate is caused by the memory buffer size used in the A-D program. The Raytheon converter is capable of up to 48 Khz sampling rates. The HP 3030 nine-track digital tape will transfer rates to 30 Khz between the computer and tape unit. However, the actual throughput rate will not equal the actual word transfer rate of the tape unit because of the overhead time necessary for writing the interrecord gaps on the tape. Hence, throughput rates are dependent on the amount of data transferred from a storage buffer, i.e., reducing the proportion of overhead time to date transfer time (storage buffer) increases the throughput rates. Table 2.5 provides the relationships between throughput rates and data buffer size. Since the buffer size used in the A-D program is 1500 words, a maximum of 23 Khz throughput rate is obtainable.

(2) System resolution is one part in 4,096 or 11 bits plus sign bit (± 2048).

(3) System accuracy is ± 1/2 of the least significant bit or ± 0.015 percent of full scale.

(4) Maximum analog inputs is eight input channels.

(5) The system provides full-scale output for analog input signals of ± 5 volts (peak-to-peak).

(6) Conversion control may be from manual, program, or external control.

TABLE 2.5. TAPE WRITE OVERHEAD

Buffer Size, 16-Bit Words	Record Write Time, μ sec	Throughput Maximum, Khz
1,000	47.7	20.5
1,500	64.3	23.0
2,000	81.0	24.0
2,500	97.7	25.0

CHAPTER 3. HARDWARE - IPLM

As indicated in Chapter 2 the interface patch logic module or IPLM is used for interfacing the analog data and command signals to the A-D converter and positive logic duplex register. Included also in this unit is self testing logic for insuring proper command signal operation. Figures 3.1 and 3.2 show the front and back views, respectively, of the IPLM. The IPLM provides the following:

(1) A patching network to patch the analog data channels to the proper converter input channels. The patching network consists of a set of BNC connectors, with the eight analog input and voice channels connected to the upper set (Fig 3.2), and the eight analog output channels to the Raytheon multiverter on the lower set. Patching is thus accomplished by connecting the selected upper set of inputs to the desired lower set of outputs.

(2) Command information to the positive logic duplex register. Outputs from the begin/end conversion switch and the begin convert sync signal are transmitted to the positive logic duplex register. The begin/end conversion signal is initiated by a single-pole, single-throw switch, normally open to signal input and normally closed to ground. The begin convert sync signal is initiated by an external signal source (0 to 1 volt = 0; 2 to 12 volts = 1). Both signals are changed to the proper logic levels for interface to the positive logic duplex register (0 volts = 1; 8 to 12 volts = 0) on lines 0 and 1.

(3) A flag signal to signify data that is to be sent. A flag signal accompanies the data lines to signal the computer that data are ready to be received. Figure 3.3 depicts the flag-data timing sequence. As noted from this figure, the flag signal accompanies both the begin and end conversion signals; however, it only accompanies the positive portion of the begin convert sync signal.

(4) Self-test logic. A test light is provided to check proper command and flag signal operations. The light is turned on by a reset switch on the front panel (see Fig 3.1). The flag signal, generated by either the begin/end conversion switch or the begin convert sync switch, turns off the light if it is sent properly. A test switch is provided which sends the begin/end conversion signal through the begin convert sync logic for checkout of the begin convert synchronizing circuitry. Use of the flag-light operation is as described in Item 3 above.

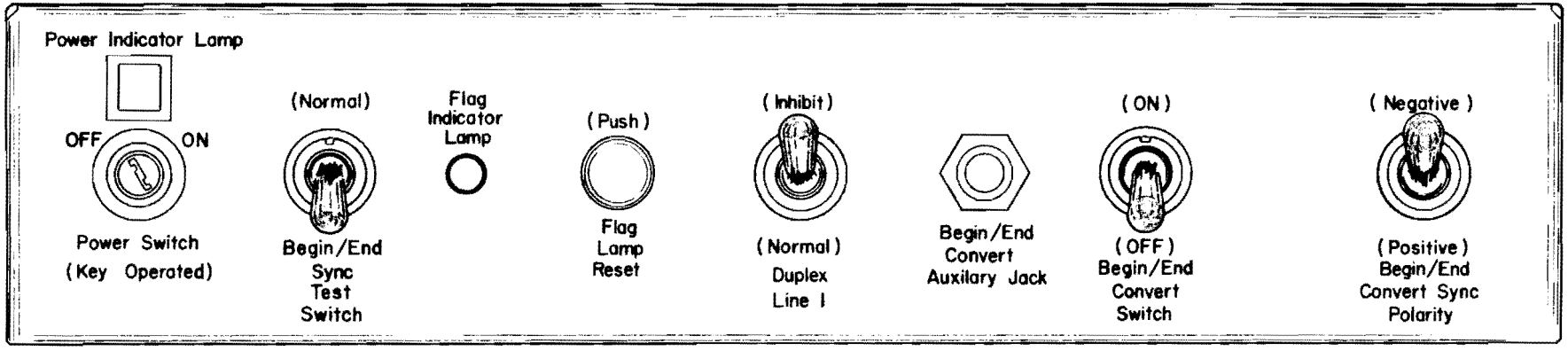


Fig 3.1. Front view of IPLM.

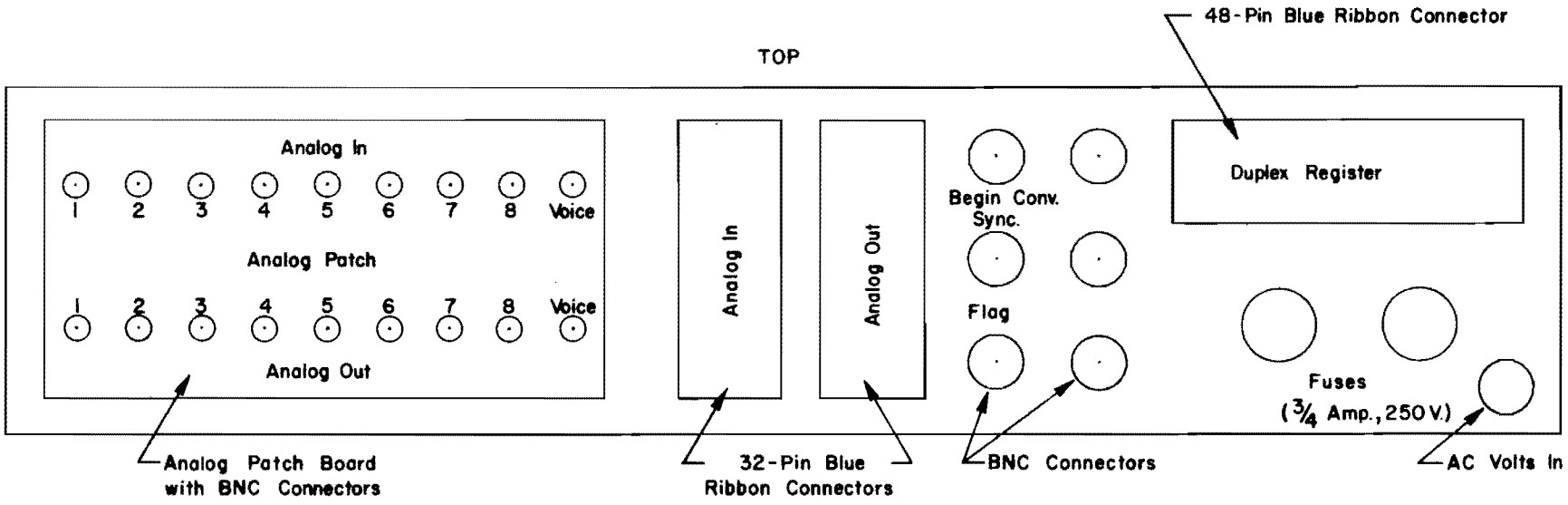


Fig 3.2. Back view of interface.

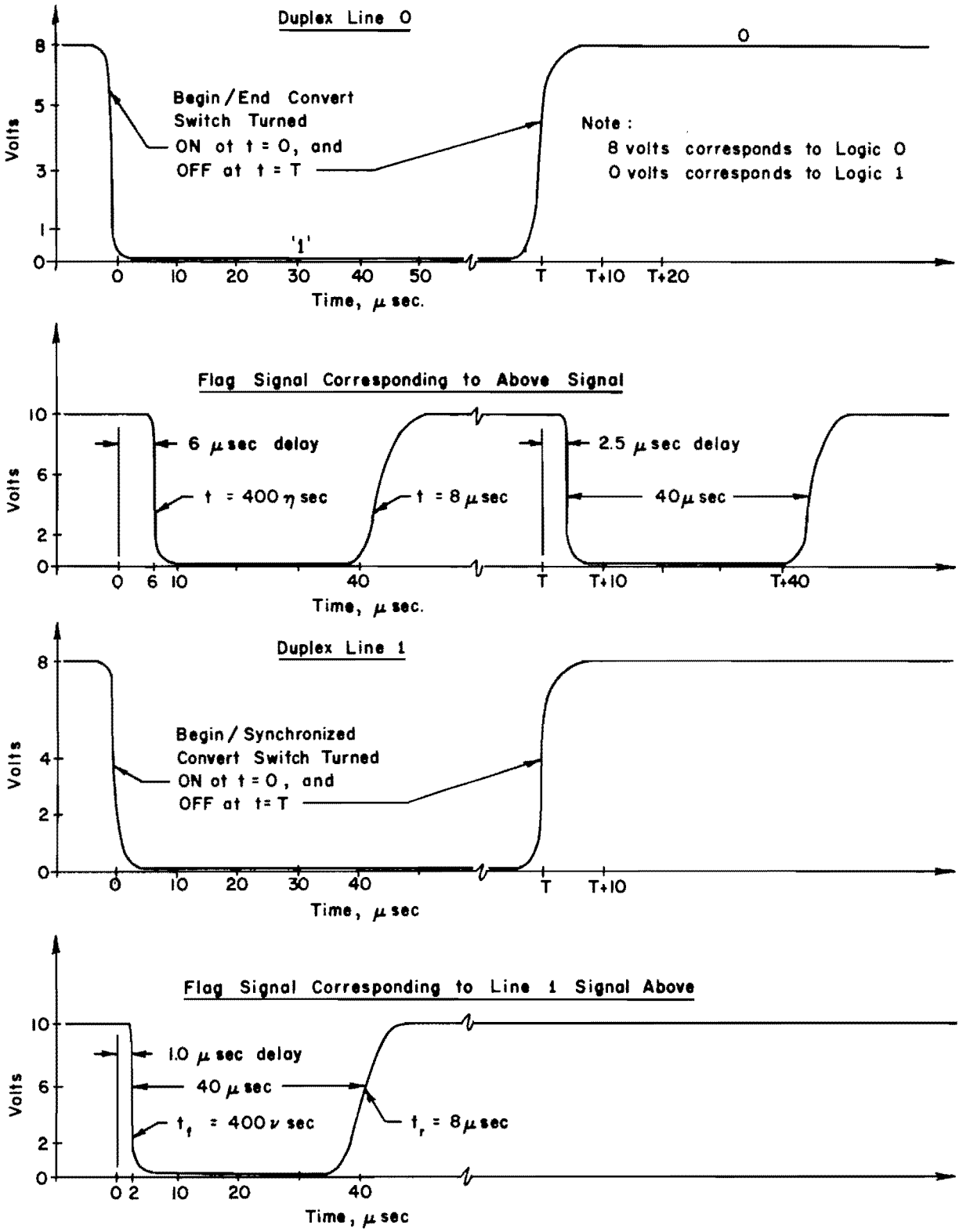


Fig 3.3. Timing diagram.

Circuit Description

A block diagram of the IPLM as depicted in Figs 3.4 and 3.5 provides the IPLM circuit schematic. Table 3.1 describes the functions of each of the switches on the unit. Command information is provided in the upper portion of Fig 3.4. The analog data input-output patching network is shown in the lower portion of the figure. The patching network can also be used for connecting the desired external begin convert sync signal to the proper circuit input and for patching the sampling signal to the multiverter.

The circuit consists of three flip-flops (FF), a number of inverters and/or circuits, a level changer, and a one shot. The begin/end convert FF shown is used to control switch bounce from the begin/end convert signal. The output from the begin/end convert FF is transferred directly to the duplex register line 0 and to the one shot via a FF delay for generating the flag signal. Both a positive and negative going signal trips the flag so the computer may be notified when the A-D conversion both begins and ends. A test switch relays the begin/end convert FF via the begin convert sync signal circuitry and places the proper begin convert sync signal on duplex line 1. As noted, this circuitry initiates a flag only on a positive going pulse. The test switch permits a checkout procedure for the begin convert sync circuitry. The level changer depicted, permits the generation of the begin convert sync signal and corresponding flag signal on either a negative or positive logic input signal.

A test light FF was included which turns off a small test light when the flag signal is generated. The light may be turned on by a reset switch which resets the test light FF.

The logic may easily be changed for the begin convert sync signal so that the flag is sent both for a positive and negative going signal as in the begin/end convert signal by adding another input to the one shot or gate. Similarly, as additional lines are used, the one shot can be wired accordingly for desired generation of the flag signal.

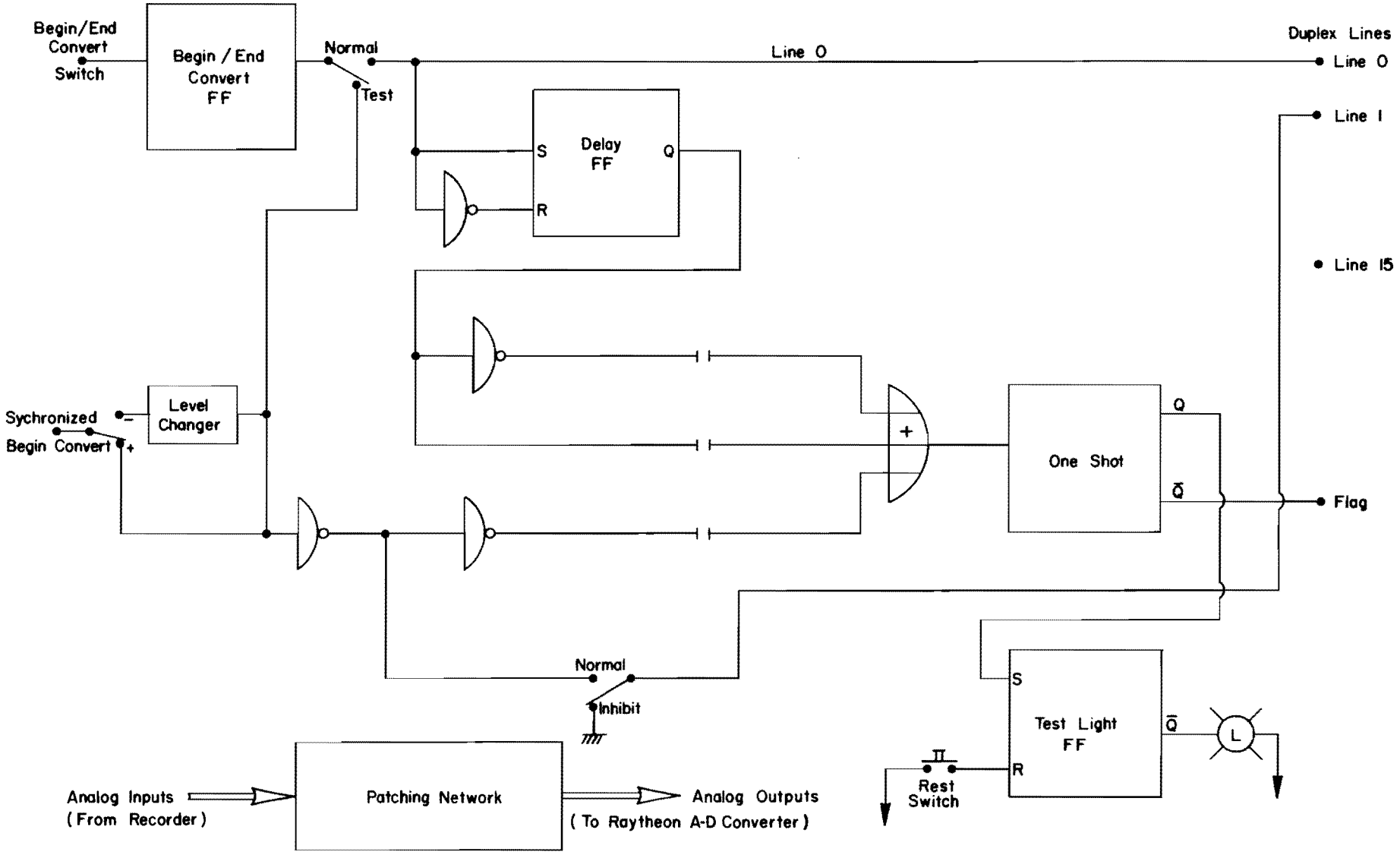


Fig 3.4. Block diagram of interface logic module (IPLM).

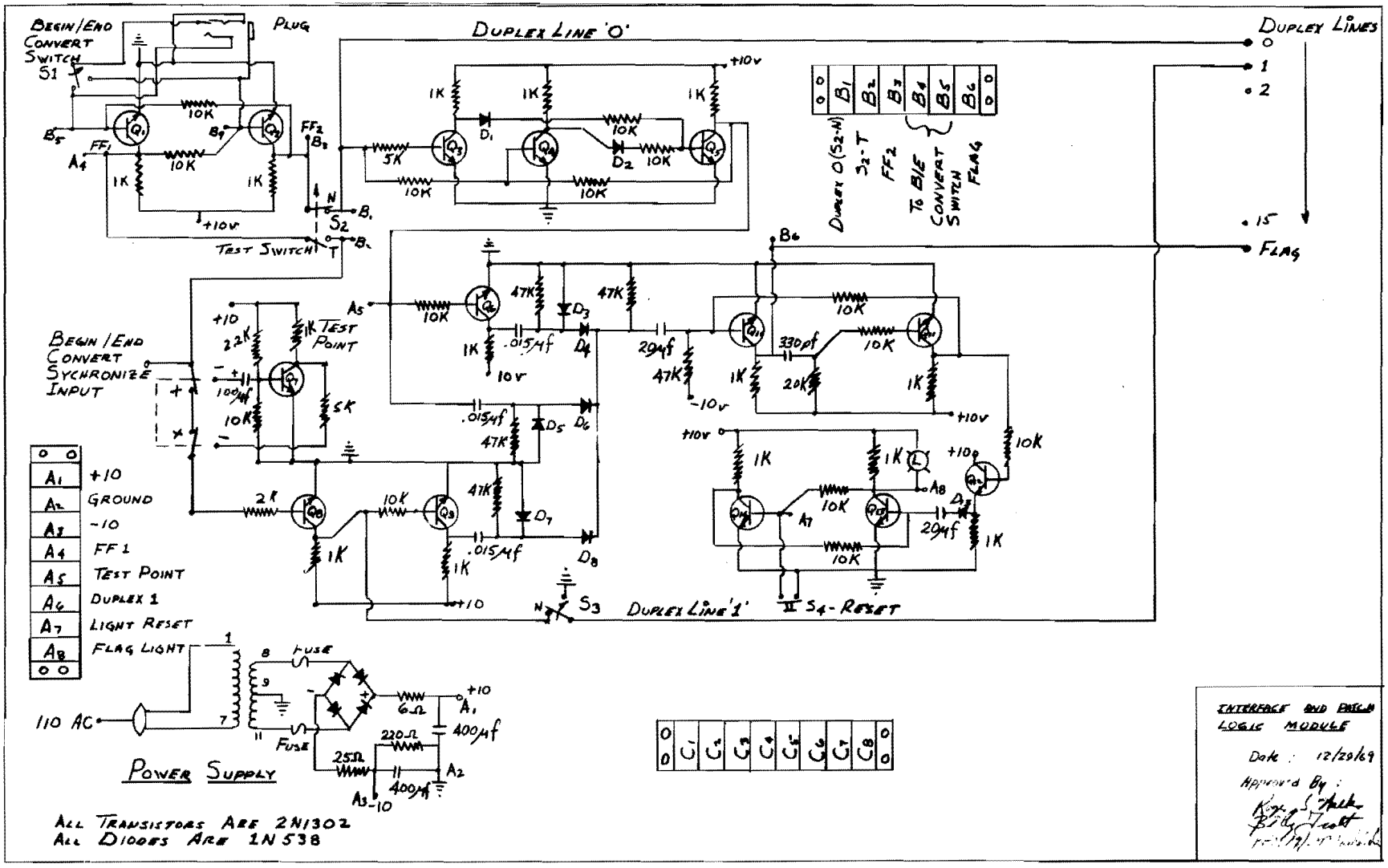


Fig 3.5. IPLM circuit schematic.

TABLE 3.1. DESCRIPTION OF INDICATORS AND CONTROLS

(1) Power Switch - When switch is on, power indicator lamp lights and operating voltage is applied to all logic circuits. Power is removed by turning switch to off position.

(2) Test Switch - When switch is in normal position, unit operates normally and duplex line 0 signal and corresponding flag signal may be tested. When switch is in begin/end convert sync position duplex line 1 signal and corresponding flag signal may be tested. The begin/end convert sync polarity switch must be in positive position for both tests.

(3) Flag Indicator Lamp - Lamp lights when flag indicator circuit is set to indicate transmission of a flag signal. When a flag signal is then transmitted the lamp is turned off.

(4) Flag Lamp Reset Pushbutton - Pushbutton is pressed to set flag indicator circuit, thereby lighting flag indicator lamp.

(5) Duplex Line 1 Switch - When the switch is in normal position, duplex line 1 is controlled by the begin/end convert sync input, i.e., when the input goes above 2 volts (positive mode) or below -2 volts (negative mode), the duplex line 1 goes from 10 volts to 0 volts (logic 0 to logic 1). When the switch is placed in the inhibit position, duplex line 1 remains at logic 1 (0 volts) regardless of inputs.

(6) Begin/End Convert Auxiliary Jack - provides remote control capabilities. Jack is connected in parallel to the begin/end convert switch with a cut-out that disables the begin/end convert switch when a phono plug is inserted into the jack.

(7) Begin/End Convert Switch - When switch is in on position, duplex line 0 becomes a logic 1 (0 volts) and the A-D converter is allowed to begin converting as soon as the synchronizing signal occurs. If duplex line 1 is inhibited, conversion begins when switch is turned to on position. Placing the switch in the off position forces duplex line 0 to logic 0 (10 volts) and stops the A-D converter.

(8) Synchronized Begin/End Convert Polarity Switch - allows use of either positive or negative begin/end convert sync signal. In the positive position, the signal must go from 0 to +2 volts, and in the negative position, the signal must go from 0 to -2 volts to set duplex line 1 to a logic 1 (0 volts).

Programming

Since the IPLM generates the proper flag signal when data are to be received by the computer, data input via both interrupt processing or "skip if flag set" sensing is possible.

The following illustrates a typical data input program through the positive logic duplex register using the assembler language.

Main program for input:

Operation	Operand	Comments
.		
.		
.		
JSB	INPUT	Jump to input subroutine
STA	CODE	Store A-register contents in memory location CODE

Input Subroutine. Commands the external device (duplex register) to acquire and transfer 16 bits of information (only two bits currently used, i.e., the begin/end conversion bit 0 and the synchronized begin convert bit 1) to the computer. Results are left in the A-register.

Label	Operation	Operand	Comments
INPUT	NOP		Entry point
	STC	GPR	Encode external device to perform its function
	SFS	GPR	Are data ready from IPLM
	JMP	*-1	No, jump to previous instruction (no data ready yet)
	LIA	GPR	Yes, data ready, transfer input data to A-register
	JMP	INPUT, I	Jump to main program

Check-Out Procedures

The IPLM check-out procedures are as follows:

(1) Isolate interface.

(2) Turn on power.

(3) Place test switch in normal position.

(4) Place duplex line 1 switch in normal position.

(5) Place begin/end convert sync polarity switch in positive position.

(6) Connect one oscilloscope channel to duplex line 0 (on back of unit - pin No. 1 of duplex register plug).

(7) Connect another oscilloscope channel to the flag signal (BNC connector on back).

(8) Set the time base to about 5 μ sec/div and vertical amplifiers to 5 volts/div.

(9) Observe both signals simultaneously as they are triggered by the duplex line 0 signal (negative).

(10) Press flag light reset to light indicator light.

Line 0 Check-Out

(11) Switch the begin/end convert switch from "Off" to "On."

Observe that the duplex line 0 should be initially at 10 volts (± 2.5) and go to 0 volts when the begin/end convert switch is turned on. After the signal of duplex line 0 has dropped, the flag signal should go from 10 volts to 0 volts (fall time = 400 η seconds). The flag signal should stay at 0 volts for about 40 μ seconds and then return to 10 volts (see timing diagram). The flag indicator light should have gone out, indicating the flag signal occurred.

(12) Reset flag light.

(13) Change the triggering of the oscilloscope to positive slope and switch the begin/end convert switch to "Off."

Observe that the duplex line 0 should be at 0 volts and go to 10 volts when the switch is turned off. When the duplex line 0 signal has reached 10 volts (± 2.5) the flag signal should occur, going from 10 volts to 0 volts (fall time = 400 η seconds). The flag signal should stay at 0 volts for about 40 μ seconds and then return to 10 volts. Again the flag indicator light should have gone out (see timing diagram).

(14) To repeat, start at Step 10.

Line 1 Check-Out

(15) Move test switch to begin/end sync position.

(16) Connect one oscilloscope channel to duplex line 1 (on back of unit - pin No. 2 of duplex register plug).

(17) Connect other channel to the flag signal (BNC connector on back).

(18) Set time base to 5 μ sec/div and vertical amplifiers to 5 volts/div.

(19) Trigger both signals by duplex line 1 (negative).

(20) Press flag light reset to light indicator light.

(21) Switch begin/end convert switch from "Off" to "On."

Observe that the duplex line 1 should be initially at 10 volts (± 2.5) and go to 0 volts when the begin/end convert switch is turned on. After the signal on duplex line 1 has dropped to 0 volts (± 2.5), the flag signal should go from 10 to 0 volts (fall time = 400 n seconds). The flag signal should stay at 0 volts for about 40 μ seconds and then return to 10 volts (see timing diagram). The flag indicator light should go out.

(22) Reset flag light.

(23) Change the oscilloscope triggering to positive slope and switch the begin/end convert switch to "Off."

Observe that the duplex line 1 should be initially at 0 volts and go to 10 volts when the switch is turned off. The flag signal should remain at 10 volts during and after this change and the flag light should not go out (see timing diagram).

(24) To repeat, start at Step 20.

Negative Begin/End Convert Sync

(25) Change begin/end convert sync polarity switch to "Negative" position.

(26) Change test switch to "Normal" position.

(27) Leave oscilloscope connected as stated in Steps 16 and 17.

(28) Use the begin convert sync BNC (on back) as an input for a negative signal. Let 0 volts correspond to the begin/end convert switch "Off" position and -10 volts (± 2) correspond to the begin/end convert switch "On" position. Note: the signal must be free of switch bounce.

(29) Perform Steps 20 through 23.

(30) To repeat, do Step 20.

Figure 3.6 provides a flow chart for the IPLM check-out procedure. Note: when duplex line 1 switch is in "Inhibit" position, duplex line 1 is always 0 volts.

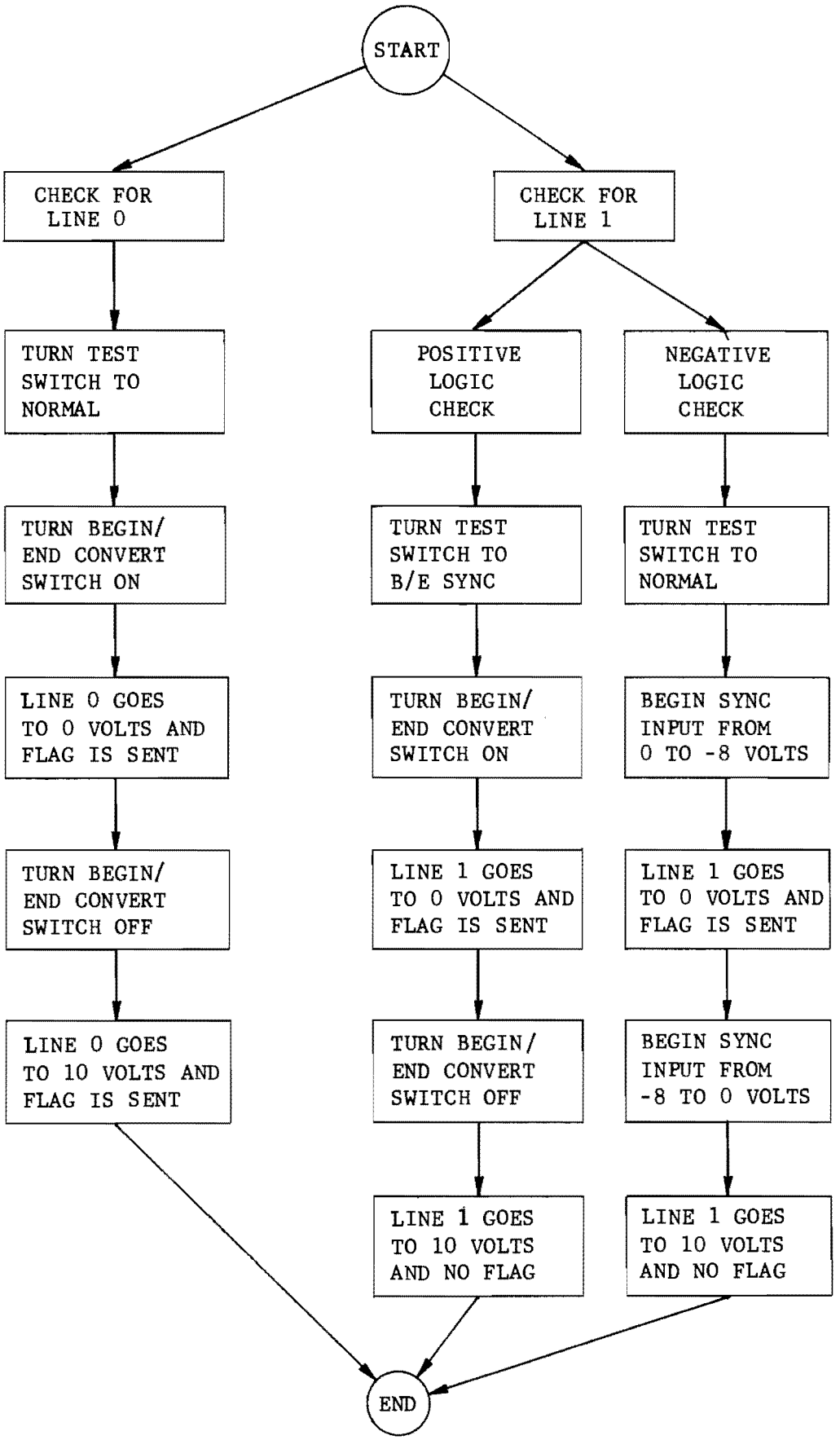


Fig 3.6. The IPLM check-out procedures.

CHAPTER 4. SOFTWARE

Two programs are required for A-D operation. The first (SAMP) is used during the actual digitizing process when the analog data are digitized and written on the nine-track tape. The second program (SERVICE) then converts the nine-track data to the standard SDS A-D format as established by earlier A-D operations (see Research Report No. 73-2) and rewrites it on a seven-track tape. The second program (SERVICE) also provides a check for parity errors which may have occurred during the first write operation as well as provides printout options for system checkout procedures.

Both the general flow of the data conversion program and the operating instructions were purposely made similar to the data conversion program used on the SDS system. This helps to maintain compatibility and ease in operation transitions from one machine to the other.

Data Conversion Program

The data conversion program SAMP is used during the A-D conversion process to provide the following functions:

(1) initiate and terminate the A-D process via external commands from the operator and/or external signals from the IPLM,

(2) read the digitized analog data at externally controlled sampling rates and writes it on the nine-track high-speed tape unit in 1500 word records at 800 bpi,

(3) write a five-word identification and end of file mark at the end of the A-D operation as signified by the begin/end convert signal, and

(4) search for a given file for replacement or search to the end of the last file for tape continuation.

A general flow chart of the data conversion program is depicted in Fig 4.1. Both FORTRAN and Assembler languages are used in the A-D program. Briefly, the general flow of the program is as follows:

(1) The program is loaded and the operator enters various operation parameters, such as

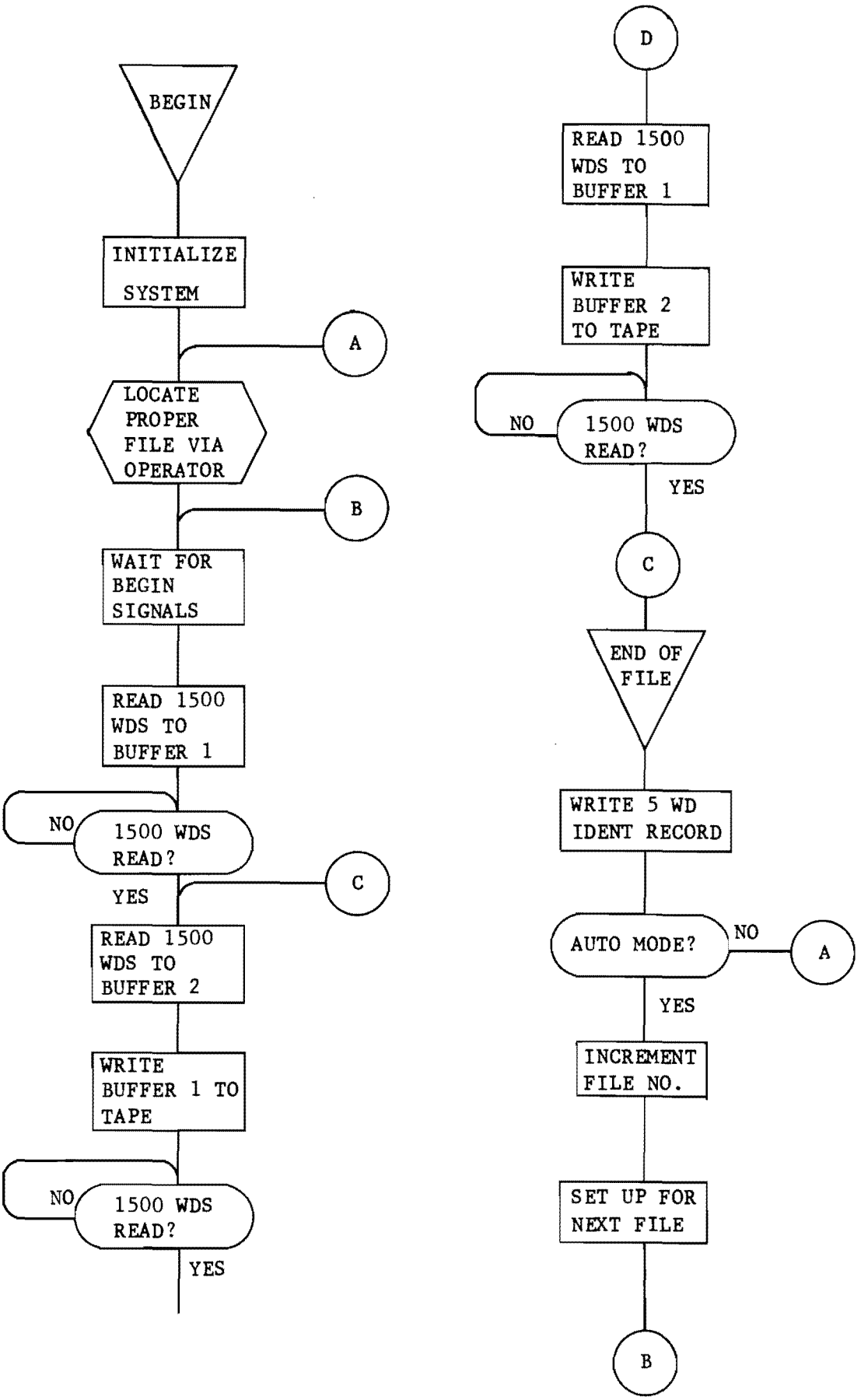


Fig 4.1. Analog-to-digital program for SDS computer.

(a) Whether a new or old data tape is used. If the tape is a new data tape, an EOF is written and the tape positioned after the EOF mark. If the tape is not a new data tape, the last data file or any other specified file is located and the tape is positioned to begin after that file.

(b) File identification information. Three words of the five-word identification code that accompany each data file is entered, i.e., the file number and the two identification tags.

(2) The program waits for the begin convert and/or photocell signal command (begin convert sync signal) to initiate the A-D process.

(3) The program uses two 1500-word buffer areas so that one buffer is being filled by the A-D input operations while the other is emptying on the magnetic tape.

(4) A new read command is immediately initiated after 1500 words have been read to insure the required sampling rate is maintained.

(5) The 1500 12-bit words in Buffer 1 are written in binary on the magnetic tape.

(6) The procedure is repeated, i.e., the filling and empyting of alternate buffers from the A-D unit to the magnetic tape continues until the end of the analog record or section being converted is detected.

(7) The conversion process is terminated by the sensing of the end conversion signal when the analog record has been completed. A five-word identification record is written at the end of the last data record. If the next analog record is to be read soon after the end of the last record and no additional identification information is desired, i.e., if the automatic control mode was specified, the program automatically increments the data file number and waits for the next begin conversion command. If not, or if other identification is required, the program stops and waits for further information or commands from the operator.

(8) Each data set (data records plus identification record) is separated by an end of file. Two ends of file are written at the end of the last data set on the magnetic tape.

Each data set or file has an identification record generated during the A-D process, which includes

(1) a data file number used by the program for identification and positioning of the data tape when adding, replacing, or deleting additional data files;

(2) the number of converted 1500-word records in the data file;

(3) the number of converted data words in the last record; and

(4) and (5) two 12-bit identification tags for additional operational information such as filter-speed-gain selection and data.

The converted data are written on the nine-track tape in the format depicted in Fig 4.2,

Figure 4.3 depicts the flow logic for operating the SAMP program. As noted the program begins by typing the statement "Enter File Number." At this point the operator specifies where the data tape is to be located for the digitizing process. Each file is labeled by a monotonic increasing file number. The operator should type in one of the following parameter types in accordance to the tape positioning desired:

(1) 0 - new data tape. The tape is rewound, an EOF written, and the tape positioned after the EOF.

(2) -1 - old data tape. The last data file on the tape is located and the tape is positioned after the EOF mark of this last file (between the EOF of the last file and the EOF signifying the end of the data tape, see Fig 4.2).

(3) +J - where J is a positive integer, $1 \leq J \leq 2047$. The J^{th} file is located and the tape positioned at the beginning of the J^{th} data file, i.e., in front of the EOF signifying the end of the data file preceding the J^{th} file.

Once the tape has been positioned, the program types "Enter New File Number and Tag." The operator should now specify the file number of the data set that is to be generated and the accompanying two 12-bit tag-information words that may be desired. This information is written at the end of the data file in the five-word identification record as described above.

After this information is entered the program waits for the external begin conversion signals that (see Chapter 2 description) initiates the conversion process. Following the end conversion signal which ends the conversion process, the program once again requests the file locating and identifying information.

Note that the -1 parameter should be entered when building the data tape as the +J parameter is used to replace the J^{th} file and the 0 parameter locates the data file at the front of the data tape.

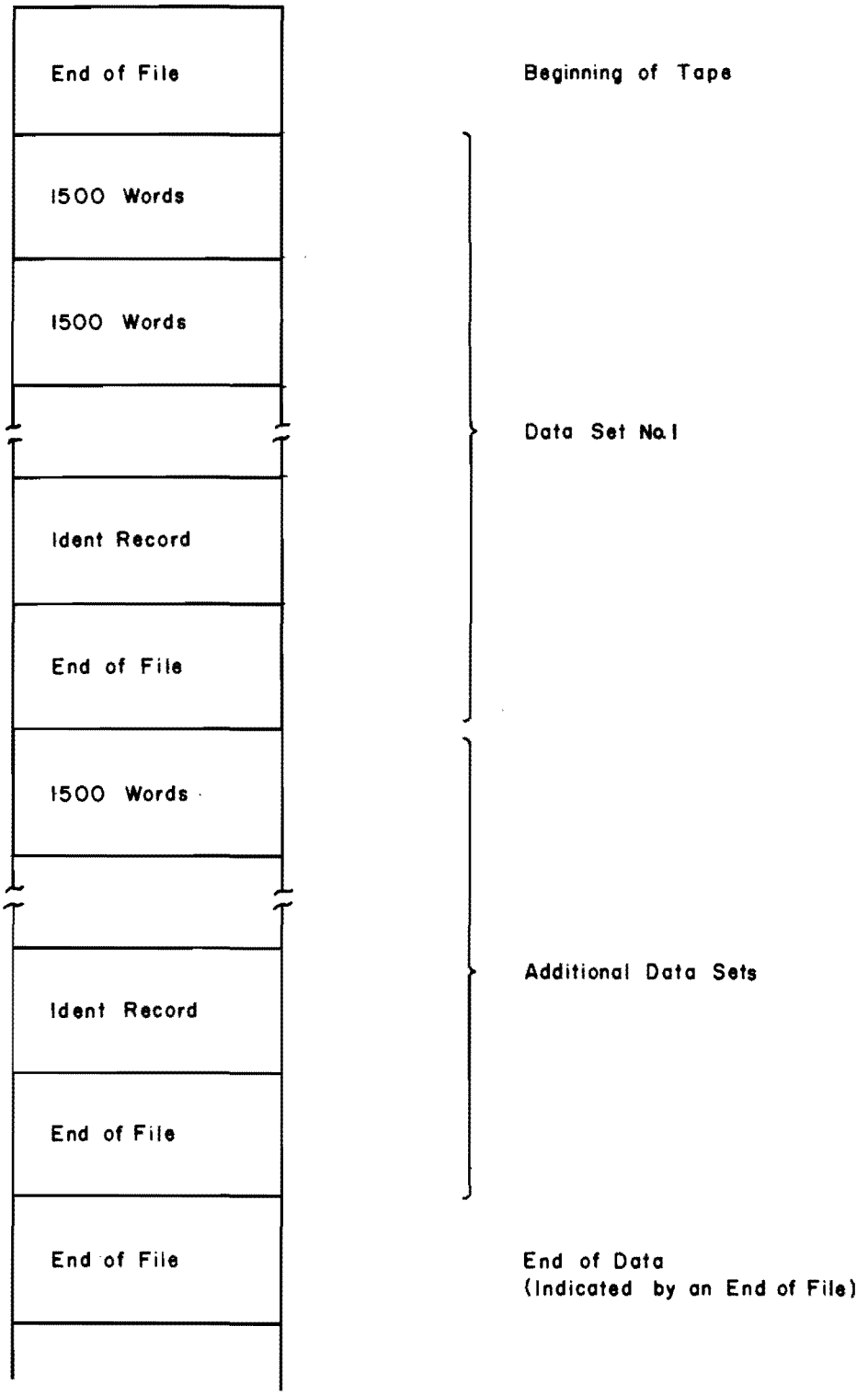


Fig 4.2. Simulated data array on digital magnetic tape.

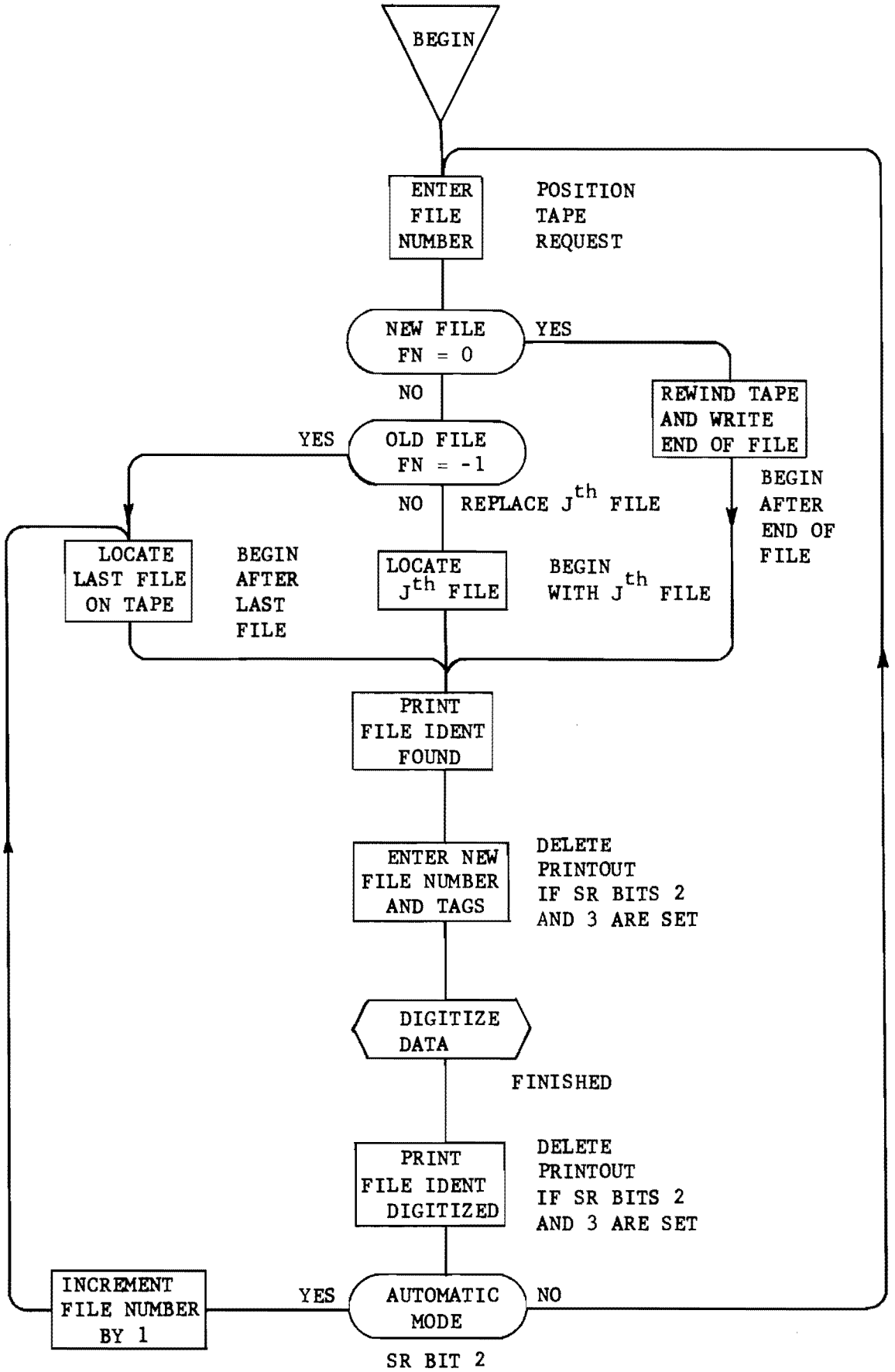


Fig 4.3. SAMP operating flow logic.

Two operating modes, manual and automatic, are used as noted in Fig 4.3. In the manual mode the above operation request is required for each data set. In the automatic mode, selected by switch register bit 2, control does not return to the operator after a data file is written. Instead, the data file number is incremented by one, and this new number is used for the next data file. The identification tags used on the previous file are also kept and the program immediately waits for the begin conversion signals. Following each data run, the file identification record is written on the teletype. When in the automatic mode, this information may be deleted by setting switch register bit 3. The error stops associated with SAMP are listed in Table 4.1.

TABLE 4.1. SAMP ERROR STOPS

Memory Location	Reason
002210	A = 11_8 ; sampling rate exceeds 23 Khz. Restart.
003060	B = 1 ; file specified cannot be located. Last file checked will be used if "Run" is depressed.
003137	B = 2 ; READ error. Depress "Run" to try READ again.

Tape Write Program

The tape conversion program (SERVICE) is used to rewrite the digitized data files contained on the nine-track tape to a seven-track tape and in a

format compatible with the SDS 930 generated data tapes. In addition, it also provides other features which enhance the A-D validation and operating procedures. The following is a description of each of the main functions provided by SERVICE:

(1) Reads the nine-track data tape (recorded at 800 bpi) and rewrites these data on a seven-track tape at 556 bpi.

   (a) The lower 12 bits of each 16-bit data words are extracted and only these lower 12 bits are written on the seven-track tape. Note that data read from the multiverter are 12 bits.

   (b) The nine-track data read from the multiverter are the negative of its true value, thus the 2's complement of these data are performed before writing it on the seven-track tape.

   (c) The SDS A-D system provides full-scale resolution for 10 volts whereas the HP system provides full-scale resolution for 5 volts. Thus, if full compatibility is specified, the data are also divided by 2 before they are written on the seven-track tape.*

(2) Lists the idents of the data files on the nine-track data tape on the teletype.

(3) Lists the digitized voltage values of the data files from the nine-track data. Included in this list are the options to:

   (a) skip through the data within a 1500-word data record,

   (b) skip through the data records within a data set file, and

   (c) skip through data files within the data tape.

(4) For generating a seven-track tape, listing data file idents or listing the digitized data values, a file-searching feature for the nine-track tape, and an automatic operating mode is also provided.

---

* The Raytheon multiverter normally provides 10-volt full-scale resolution but was modified in accordance with project specifications to be more compatible with the signal amplitudes most commonly used by current research projects. This compatibility feature is not needed when digitizing road profile data as scaling is relative to 1-inch calibration factors. Thus, for these data the HP system provides a two-fold increase in resolution over the SDS system.

(a) The file-searching procedure is provided in SERVICE so that any given file on the nine-track tape may be specified. For example, when building a seven-track tape, only selected files need be included.

(b) An automatic mode is provided when using SERVICE so that each file on the nine-track tape is processed automatically in sequential order. For example, when building a seven-track tape, the operator only needs to specify the first file on the nine-track tape. The remaining files are automatically processed in the order contained on the nine-track tape.

Figure 4.4 provides a general flow chart of the SERVICE program. The general flow depicted in this figure is as follows:

(1) The program begins by indicating its beginning and if desired, provides a list of the switch register functions.

(2) The program asks for the nine-track data file number. If a file number of zero or less is specified, the first file on the data tape is found. Otherwise the file number specified is located and the five-word identification record is printed for this file.

(3) If switch register bit 15 is set used for listing data file idents, the program repeats back to Step 2. If the automatic mode is selected, the ident number of the next data file on the data tape is found, listed, and the process repeated. If the automatic mode is not specified, the program asks the operator for the file desired and the program repeats Step 2.

(4) If switch register bit 14 is set, the program writes a seven-track data tape. The first time the tape write routine is entered the 10 or 5-volt resolution is specified by the operator. The program then writes an end of file on the seven-track tape (see tape format, Fig 4.2).

(5) The program begins reading the nine-track tape and writing the seven-track tape (multiplying each data word by -1, and if the 10-volt resolution is specified, dividing each word by 2).

(6) The automatic and manual modes operate as described in items 2 and 3 above with switch register bit 14 used to route the program flow to the tape write subroutine as depicted in Fig 4.4.

(7) If switch register bit 13 is set, the program lists the nine-track data tape. The data words listed are scaled to volts for checkout purposes. Three skip options are available: skip through the data record (switch register bit 1), skip through the data set (switch register bit 3), and skip through the data tape (switch register bit 4). The program reads one record at a time, scales the data, and begins printing it on the teletype. By setting switch register bit

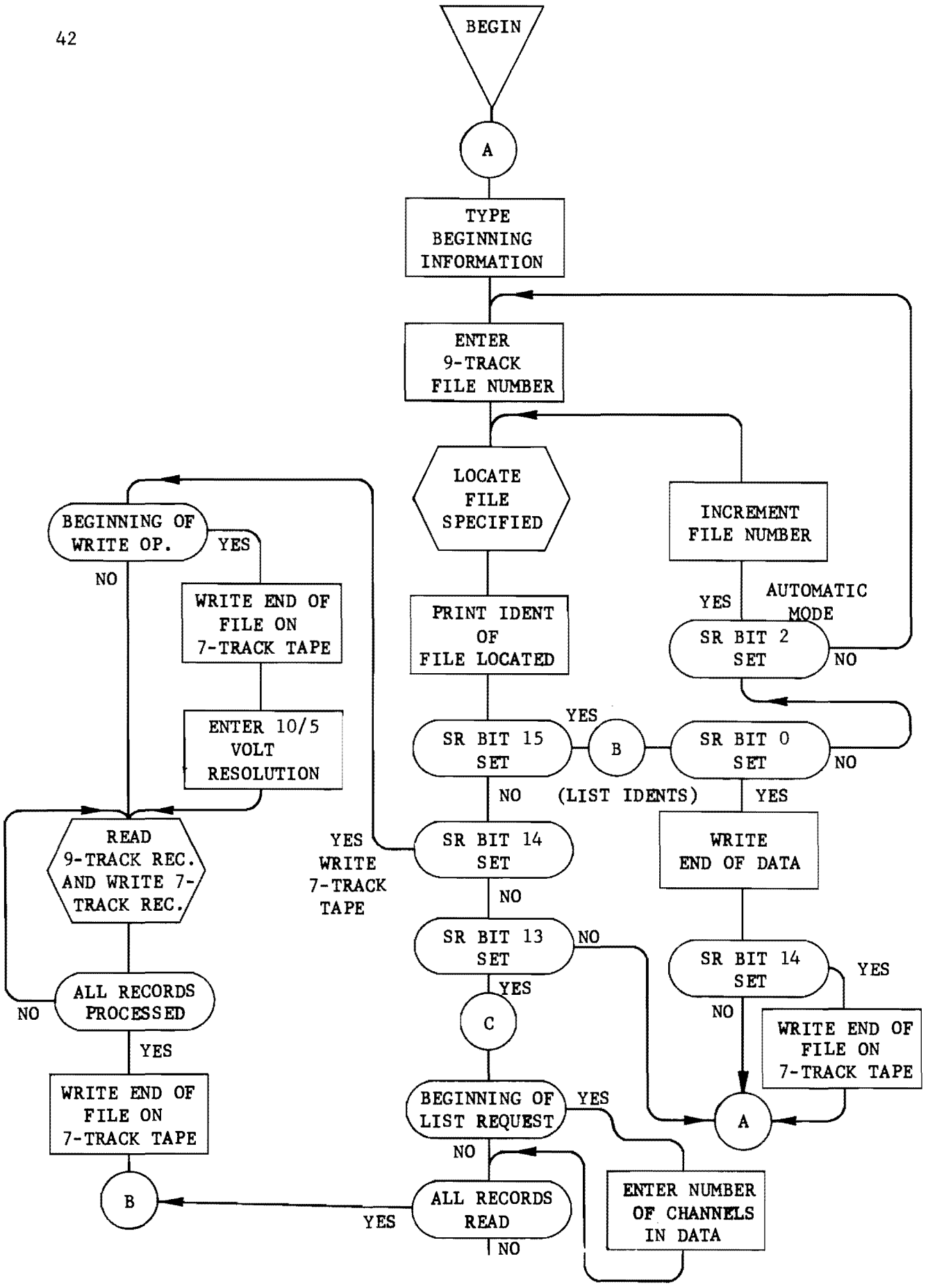


Fig 4.4. Service flow chart (continued on next page).

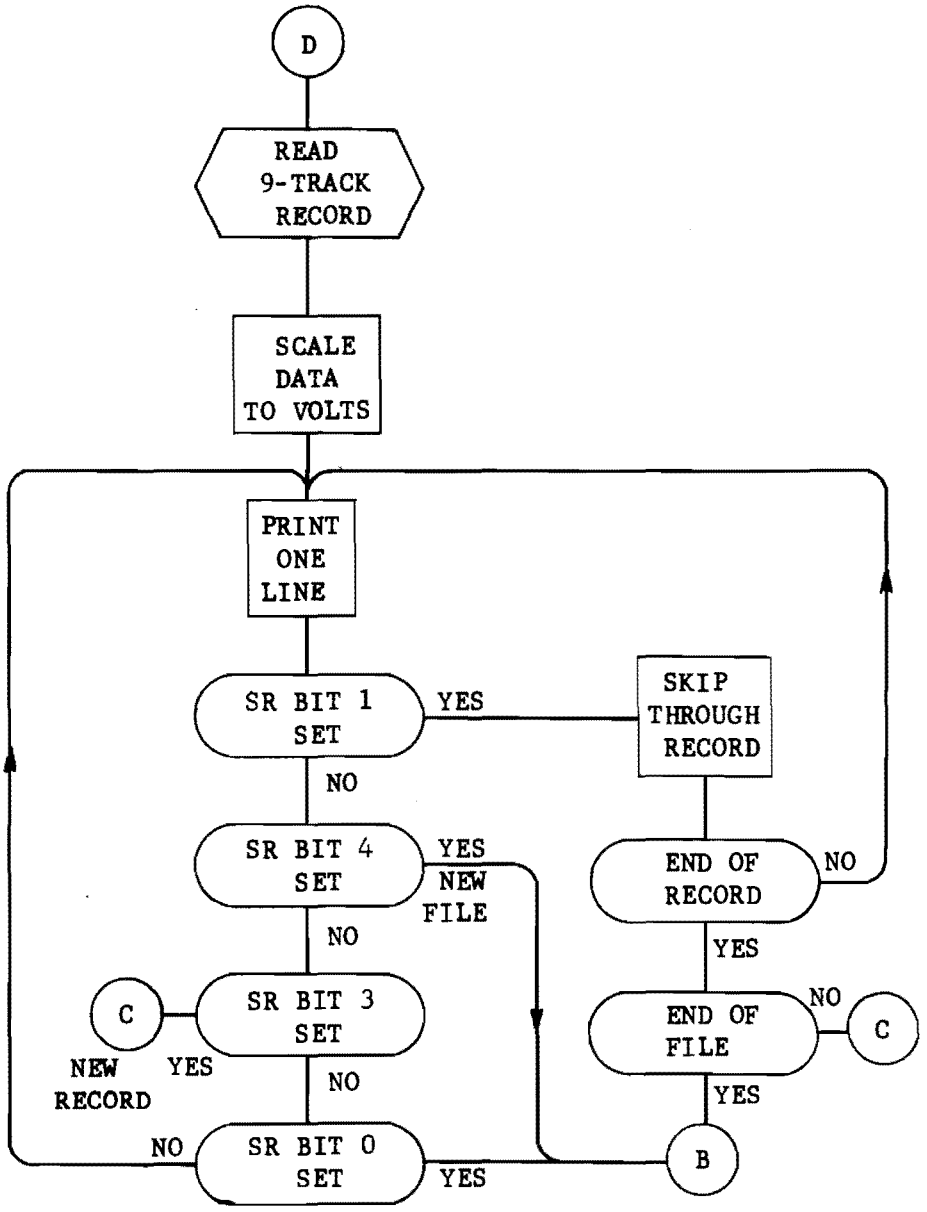


Fig 4.4. (Continued from previous page).

1, the programs delete the printout until the switch register bit 1 is cleared. Switch register bits 3 and 4 work similarly for skipping records and files, respectively. The data are printed on each line of the teletype in the channel order digitized, where the number of channels digitized is entered at the beginning of the list program.

(8) The automatic and manual operation works similar to that described in Items 3 and 4 above where switch register bit 13 routes the program flow to the list subroutine as depicted in Fig 4.4.

Table 4.2 provides a listing of the error stops in SERVICE.

TABLE 4.2. SERVICE ERROR STOPS

Memory Location	Reason
004274	$A = 24_8$; HP 3030 unit in motion or in "Local." Set unit. Press "Run."
004314	$A = 25_8$; Parity error on HP 3030 unit. Press "Run" will use data with error(s).
004317	$A = 26_8$; I/O command rejected on HP 3030 unit. Run diagnostics on tape unit.

CHAPTER 5. OPERATING PROCEDURES

This chapter provides a description of the operating procedures used to perform A-D operations in accordance with the system described in this report. The procedures are divided into two areas: system setup procedures and general operating procedures. Also included at the latter part of the chapter is a brief description of some checkout procedures for A-D validation.

System Setup Procedures

The following items are required for A-D operations:

(1) HP 2115 system as specified in Fig 2.2;

(2) interface and patch logic module (IPLM) as shown in Fig 2.5;

(3) input voltage source such as Honeywell Model 8100 analog tape;

(4) two digital tapes, preferably one certified at 3200 bpi for the nine-track tape and the other at 800 bpi for the seven-track tape;

(5) seven-track operating tape prepared for the A-D system (A-D program tape);

(6) all necessary cables for patching the analog signals (coaxial cables with BNC connectors on both ends); and

   (a) recorder - IPLM cable, 12-foot cable with Winchester plug on the recorder end and a 16-pin Blue Ribbon connector on the IPLM end,

   (b) IPLM - Computer cable, 12-foot cable with a 32-pin Blue Ribbon connector on the IPLM end and the 16-bit positive logic duplex output plug on the computer end, and

   (c) IPLM - Multiverter cable, 12-foot cable with a 16-pin Blue Ribbon connector on the IPLM end and the analog input connector on the multiverter end.

(7) oscilloscope.

The following setup procedures (see Fig 5.1) should then be used for setting up the system:

(1) The computer, teletype, tape units, pulse generator, multiverter, IPLM, and oscilloscope should all be turned on.

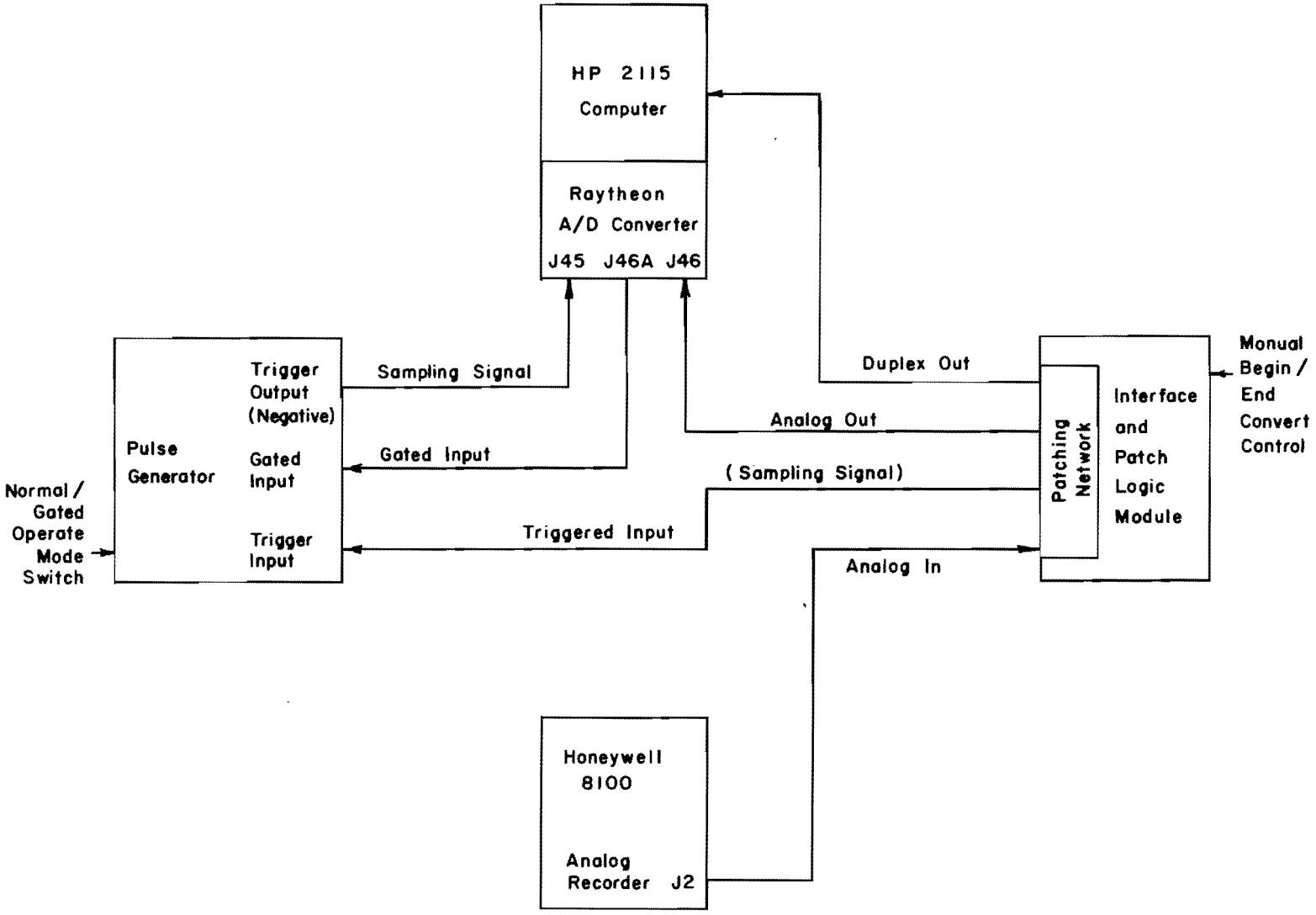


Fig 5.1. Cable interconnection diagram.

(2) The IPLM - Computer cable should be connected from the IPLM unit to the positive logic duplex card (Duplex Out, Fig 3.1).

(3) The IPLM - Multiverter cable should be connected to the IPLM and the J46 plug on the back of the Raytheon multiverter (Analog Out, Fig 5.1).

(4) The recorder - IPLM cable should be connected between the Honeywell 8100 analog recorder pin J2 and the analog in connector on the IPLM.

(5) The desired analog channels to be digitized (upper set of BNC connectors, Fig 3.2) should be patched to the multiverter input channels (lower set of BNC connectors, Fig 3.2).

(6) (External sampling signal option only.) The external sampling signal should be connected from the analog in patch BNC connector to the trigger input terminal of the pulse generator.

(7) A cable should be connected between the trigger output (negative) on the pulse generator to pin J45 on the multiverter. A BNC T connector should be used at the pulse generator output for monitoring the sampling signal (Sampling Signal, Fig 5.1).

(8) A cable should be connected between the gated input connector J46A on the back of the multiverter (Gated Input, Fig 5.1).

(9) (External begin convert sync signal option.) Connect a cable between the proper analog input connector and the begin convert sync BNC connector (see Fig 3.2).

(10) Insure jumper W6A in the negative logic duplex registers card has been removed.

(11) Set the Raytheon multiverter in the normal mode, select the sync external switch, and select the number of conversion channels.

(12) Set the normal/gated switch in the back of the multiverter to "Normal" for checking the pulse characteristics.

(13) Set the pulse generator to internal and adjust the pulse amplitude to about 5 volts. Adjust the pulse width to 5 μ. If the sampling signal is generated from the pulse generator, set the sampling rate in accordance with Eq 2.1.

(14) Set the normal/gated switch to the gated position in back of the pulse generator.

(15) Set the IPLM as follows:

  (a) Test switch in "Normal."

  (b) Duplex line in "Connect" position if an external begin convert sync signal is provided, otherwise set in "Inhibit" position.

  (c) Set the begin/end convert switch to "Off."

d. Set the begin connect sync polarity switch to "+" for positive logic and "-" for negative logic.

(16) Mount the nine-track data tape and seven-track operating system program tape.

(17) Load A-D program, Ident 500*.

(18) Program types "Enter File Number."

Enter 0 for new data tape

-1 for old data tape

+J when J is a positive integer for replacing J^{th} file, (see Chapter 4).

(19) Program types "Enter New File Number and Tag." Enter file number of data file and ident tags (see Chapter 4).

(20) Program is now waiting for the begin convert and begin convert sync signals. Switch register bit 2 signifies automatic mode and should be set at this time if desired. Switch register bit 3 inhibits file print out information.

The system is now ready for digitizing the file number specified in Item 19 when the proper control signals are initiated.

General Operating Procedures

Two operating procedures will be described, one for the data conversion process and the second for the tape write process. The ident list and print-out list options are not described in this section but provided in detail in Chapter 4.

Data conversion process. The following procedures are those necessary for A-D operations:

(1) Two switch register bits are used, one for automatic mode selection bit 2, and the second for inhibiting file ident printout when in the automatic mode, bit 3.

(2) Two entries are required by the data conversion program for file location and file identification. The file location entry signaled by the type out, "Enter File Number," is always requested first. At this time the operator should enter the file number location of where the data tape is to be positioned for the digitizing process.

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* Both SAMP and SERVICE may sometimes be restarted by beginning at location 00002.

The following parameters are used for entering this information:

0 - new data tape. The tape is rewound, an EOF written. The tape is positioned after the EOF.

-1 - old data tape. The last data file on the tape is located and the tape positioned after the EOF mark of this last file.

+J - where J is a positive integer, $1 \leq J \leq 2047$. The J^{th} file located and the tape positioned at the beginning of the J^{th} data file, i.e., the J^{th} file will be rewritten.

The second entry signaled by the type out, "Enter New File Number and Tag," is used to specify the file number and two ident tags for the data file that is to be digitized.

(3) The operating procedure is to first specify the location on the tape for the new digitized file and then to identify this new file. The appropriate switch register bits are set and the digitizing process begun. If the automatic mode is indicated, control is not returned to the operator after the process but the program returns to monitor the input signals for the begin convert commands. If the manual mode is specified, control is returned to the operator and once again he should first specify the tape location and then the new file identification. Note that when digitizing several files the -1 parameter should be used for the file location parameter.

Tape Write Process. The following procedures are those necessary for the tape write process:

(1) Mount the nine-track data tape on the HP 3030 tape unit and the seven-track A-D system tape on the HP 2020 tape unit.

(2) Load the tape write program, Ident 501, from seven-track program tape.

(3) Remove program tape and mount the seven-track data tape on the 2020 tape unit.

(4) Press Run. The program will type "Begin Data Service Routine," and "Set SS 10 for SS List." Set switch register 14 and press Run. The computer will type "Pause." Depress Run again. The program will type "Enter File Number." The file number of the nine-track data file that is to be written on the seven-track data tape should be entered. The parameter 0 may be used if the first file on the nine-track tape is desired.

(5) The program will type "Enter 1,0 for 10,5-Volt Resolution." Enter either a 1 or 0 for 10-volt resolution, SDS compatibility or 5-volt resolution, respectively.

(6) The program writes an end of file on the seven-track tape and transfers the data file specified on the nine-track data tape to the seven-track tape.

(7) The program once again types "Enter File Number" unless the automatic mode is specified, switch register bit 2. If the automatic mode has been specified the program continues to read consecutive data files and writes these files on the seven-track tape. If the automatic mode is not desired, i.e., switch register bit 2 is not set, the next data file to be processed is entered and the process is repeated.

(8) When the last data file is being generated on the seven-track tape, switch register bit 0 should be set. If this bit is set, the program writes a second EOF mark after the data file has been written. The program then types "Begin Data Service Routine," "Set SS 10 for SS List." The service routine is then available for a new set of operations.

System Check-Out Procedures

During an A-D operation, the digitized values may be checked by loading the tape write program, Ident 501. Then by specifying the data list option (see Chapter 4) denoted by switch register bit 13, the converted data in volts may be displayed via the teletype. Switch register bit 1 may be used for skipping through the data record, bit 3 for skipping through the data file and bit 4 for skipping through the data tape. Switch register bit 2 provides the automatic mode so that consecutive files may be examined without calling for each one individually. Thus, by putting in known voltage values before an A-D operation, a quick check on the system may be obtained by checking the values digitized.

CHAPTER 6. SYSTEM CHECK-OUT PROCEDURES

To insure the A-D system could meet the system specifications and to provide an acceptable check-out procedure the following tests were set up and are described in this chapter. The tests described were made on the system during May 1969, and the results obtained provided. Such tests should be performed in conjunction with the HP system diagnostic programs periodically to insure the system is performing in an acceptable manner.

Conversion Speed and Accuracy

In order to insure the system could digitize at variable rates to 25 Khz with the specified accuracy, a test was conducted in which known inputs were digitized at variable conversion rates to 25 Khz. The A-to-D inputs were connected as follows:

(1) Channel 0 = shorted;
(2) Channel 1 = -1.520 v;
(3) Channel 2 = shorted;
(4) Channel 3 = +1.528 v;
(5) Channel 4 = shorted;
(6) Channel 5 = shorted for 850 hz test, 250 hz triangle wave (4.0 v P-P) for 25 Khz;
(7) Channel 6 = shorted; and
(8) Channel 7 = 250 hz square wave, 10.0 v P-P.

As noted from the selected computer results, Table 6.1, the digitized values are within the specified system accuracy, i.e., 12 bits ± LSB.

Further Tests on System Resolution

As a further check on system resolution for the time varying signal case, sine and triangle wave forms were sampled at 60 points per cycle by the following technique. A 20 hz sine wave of ± 2.5 v P-P was connected to channels 0, 2, and 4. Likewise, a 20 hz triangle wave of the same P-P

TABLE 6.1. CONVERSION SPEED AND SEQUENCING VALIDATION

SAMPLING RATE = 850 hz

	CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7
1	.000	-1.521	.002	1.528	.000	.000	.000	-4.995
9	.002	-1.521	.002	1.528	.000	.000	.000	-4.995
17	.002	-1.521	.002	1.528	.000	.000	.000	-4.995
25	.002	-1.521	.002	1.528	.000	.000	.000	-4.995
33	.002	-1.521	.002	1.528	.000	.000	.000	-4.995
41	.002	-1.521	.002	1.528	.000	.000	.000	-4.995

	CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7
1	.000	-1.521	.002	1.528	.000	.000	.000	5.000
9	.000	-1.521	.002	1.528	.000	.000	.000	5.000
17	.000	-1.521	.002	1.528	.000	.000	.000	5.000
25	.000	-1.521	.002	1.528	.000	.000	.000	5.000
33	.000	-1.521	.002	1.528	.000	.000	.000	5.000
41	.000	-1.521	.002	1.528	.000	.000	.000	5.000
49	.000	-1.521	.002	1.528	.000	.000	.000	5.000
57	.000	-1.521	.002	1.528	.000	.000	.000	5.000

	CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7
1	.000	-1.521	.002	1.528	.000	.000	.000	5.000
9	.000	-1.521	.002	1.528	.000	.000	.000	5.000
17	.000	-1.521	.002	1.528	.000	.000	.000	5.000
25	.000	-1.521	.002	1.528	.000	.000	.000	5.000
97	.000	-1.521	.002	1.528	.000	.000	.000	5.000
105	.000	-1.521	.002	1.528	.000	.000	.000	5.000
225	.000	-1.521	.002	1.528	.000	.000	.000	5.000
233	.000	-1.521	.002	1.528	.000	.000	.000	5.000
241	.000	-1.521	.002	1.528	.000	.000	.000	5.000
401	.000	-1.521	.002	1.528	.000	.000	.000	5.000
409	.000	-1.521	.002	1.528	.000	.000	.000	5.000

	CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7
1	.002	-1.521	.002	1.528	.000	.000	.000	-4.995
9	.002	-1.521	.002	1.528	.000	.000	.000	-4.995
217	.002	-1.521	.002	1.528	.000	.000	.000	-4.995
225	.002	-1.521	.002	1.528	.000	.000	.000	-4.995
545	.002	-1.521	.002	1.528	.000	.000	.000	-4.995
553	.002	-1.521	.002	1.528	.000	.000	.000	-4.995
561	.002	-1.521	.002	1.528	.000	.000	.000	-4.995
569	.002	-1.521	.002	1.528	.000	.000	.000	-4.995
825	.002	-1.521	.002	1.528	.000	.000	.000	-4.995

TABLE 6.1. (Continued)

SAMPLING RATE = 25 Khz

	CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7
1	.000	-1.533	.000	1.531	.000	-.466	.000	5.000
9	.000	-1.531	.000	1.531	.000	2.012	.000	-4.998
17	.000	-1.531	.000	1.531	.000	-1.433	.000	-4.998
25	.000	-1.531	.000	1.531	.000	-.112	.000	5.000
33	.000	-1.531	.000	1.531	.000	1.658	.000	-4.998
249	.000	-1.531	.000	1.531	.000	-1.528	.000	-4.992
257	.000	-1.531	.000	1.531	.000	-.015	.000	5.000
265	.000	-1.531	.000	1.531	.000	1.562	.000	-4.998
273	.000	-1.528	.000	1.531	.000	-1.882	.000	5.000
281	.000	-1.531	.000	1.531	.000	.342	.000	5.000
289	.000	-1.531	.000	1.531	.000	1.206	.000	-4.998
297	.000	-1.531	.000	1.531	.000	-2.236	.000	5.000

	CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7
1	.000	-1.531	.000	1.531	.000	-2.100	.000	5.000
9	.000	-1.531	.000	1.531	.000	1.360	.000	5.000
17	.000	-1.531	.000	1.531	.000	.186	.000	-4.998
25	.000	-1.531	.000	1.531	.000	-1.743	.000	5.000
33	.000	-1.531	.002	1.531	.000	1.716	.000	-4.995
41	.000	-1.531	.002	1.531	.000	-.168	.000	-4.998
313	.000	-1.531	.002	1.531	.000	2.473	.000	-4.998
321	.000	-1.531	.000	1.531	.000	-.972	.000	-4.998
329	.000	-1.531	.002	1.531	.000	-.579	.000	5.000
337	.000	-1.531	.000	1.531	.000	2.122	.000	-4.998
633	.000	-1.531	.000	1.531	.000	.588	.000	5.000
641	.000	-1.531	.000	1.531	.000	.957	.000	-4.998
649	.002	-1.531	.002	1.531	.000	-2.480	.000	5.000
657	.000	-1.531	.002	1.531	.000	.945	.000	5.000
665	.000	-1.528	.002	1.531	.000	.603	.000	-4.995
673	.000	-1.531	.000	1.531	.000	-2.161	.000	5.000
1073	.000	-1.531	.000	1.531	.000	.430	.000	5.000
1081	.000	-1.531	.002	1.531	.000	1.118	.000	-4.992
1089	.000	-1.531	.002	1.531	.000	-2.322	.000	5.000

	CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7
1	.002	-1.531	.002	1.531	.000	1.040	.000	5.000
9	.000	-1.528	.002	1.531	.000	.513	.000	-4.998
17	.002	-1.531	.002	1.531	.002	-2.065	.002	5.000

ALL DONE
STOP

amplitude was connected to channels 1, 3, and 5. The wave forms were then sampled at 160 hz, yielding 60 points per cycle per wave form. Selected results of this test are given in Table 6.2 and depicted graphically in Figs 6.1 and 6.2.

Test for Loss of Data

Finally, to insure each sampling pulse resulted in an actual data sample, a digital counter was connected in parallel with the pulse generator and the input to the computer. Variable length data files were then generated by use of the A-D program. The number of data points converted as indicated by the program were then compared to the number of sampling pulses sent into the system. In all cases the numbers were found to be consistent for the variable sampling rates.

TABLE 6.2. DATA RESOLUTION VALIDATION

	CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7
1	1.348	1.396	1.973	1.519	2.080	1.643	.002	5.000
9	2.258	1.899	2.332	2.014	2.335	2.136	.002	5.000
17	2.456	2.383	2.476	2.490	2.471	2.366	.000	-4.990
25	2.419	2.117	2.378	1.992	2.319	1.870	.000	-4.990
33	2.161	1.621	2.063	1.497	1.953	1.375	.000	-4.990
41	1.689	1.125	1.541	1.001	1.387	.879	.000	-4.993
49	1.057	.630	.876	.508	.688	.383	.000	-4.993
57	.365	.137	.112	-.012	-.081	-.112	.002	-4.993
65	-.466	-.359	-.659	-.481	-.847	-.605	.002	-4.993
73	-1.196	-.852	-1.368	-.974	-1.516	-1.099	.002	-4.993
81	-1.809	-1.345	-1.938	-1.467	-2.051	-1.592	.002	-4.990
89	-2.244	-1.833	-2.324	-1.960	-2.385	-2.083	.002	-4.990
97	-2.461	-2.329	-2.483	-2.454	-2.490	-2.410	.002	5.000
105	-2.451	-2.161	-2.415	-2.036	-2.363	-1.912	.002	5.000
113	-2.209	-1.663	-2.114	-1.539	-2.007	-1.414	.002	5.000
121	-1.753	-1.165	-1.696	-1.040	-1.453	-.916	.002	5.000
129	-1.123	-.669	-.947	-.544	-.762	-.420	.002	5.000
137	-.376	-.171	-.183	-.049	.210	.376	.002	5.000
145	.396	.322	.591	.447	.781	.571	.000	5.000
153	1.148	.818	1.306	.942	1.452	1.367	.000	5.000
161	1.758	1.313	1.892	1.439	2.009	1.560	.000	5.000
169	2.205	1.809	2.285	1.931	2.351	2.356	.002	5.000
177	2.437	2.302	2.463	2.424	2.488	2.449	.000	-4.990
185	2.441	2.206	2.407	2.275	2.358	1.951	.000	-4.990
193	2.219	1.704	2.129	1.580	2.026	1.455	.000	-4.990
201	1.782	1.208	1.638	1.084	1.489	.959	.000	-4.993
209	1.169	.713	.999	.588	.815	.466	.000	-4.993
217	.432	.217	.239	.095	.046	-.029	.002	-4.993
225	-.337	-.276	-.532	-.400	-.723	-.522	.002	-4.993
233	-1.086	-.769	-1.252	-.894	-1.414	-1.016	.002	-4.993
241	-1.716	-1.262	-1.855	-1.387	-1.978	-1.509	.002	-4.993
249	-2.185	-1.755	-2.273	-1.877	-2.346	-2.002	.002	-4.993
257	-2.444	-2.249	-2.471	-2.371	-2.493	-2.493	.002	5.000
265	-2.468	-2.244	-2.441	-2.119	-2.466	-1.995	.002	5.000
273	-2.263	-1.746	-2.180	-1.621	-2.080	-1.497	.002	5.000
281	-1.843	-1.248	-1.704	-1.123	-1.555	-.999	.002	5.000
289	-1.235	-.750	-1.067	-.627	-.886	-.503	.002	5.000
297	-.535	-.254	-.313	-.129	-.128	-.007	.002	5.000
305	.269	.242	.461	.364	.654	.488	.000	5.000
313	1.025	.737	1.196	.859	1.362	.934	.000	5.000
321	1.663	1.230	1.804	1.355	1.934	1.479	.000	5.000
329	2.146	1.726	2.234	1.848	2.310	1.973	.002	5.000
337	2.415	2.219	2.449	2.344	2.471	2.466	.000	-4.990
345	2.458	2.283	2.432	2.158	2.393	2.034	.000	-4.993
353	2.274	1.785	2.190	1.663	2.095	1.538	.000	-4.990
361	1.873	1.289	1.736	1.167	1.589	1.042	.000	-4.993
369	1.279	.796	1.113	.671	.938	.547	.000	-4.993
377	.562	.308	.369	.176	.176	.054	.002	-4.993
385	-.219	-.193	-.403	-.317	-.596	-.442	.002	-4.993
393	-.968	-.682	-1.145	-.811	-1.309	-.935	.002	-4.993
401	-1.619	-1.132	-1.765	-1.304	-1.897	-1.428	.002	-4.993

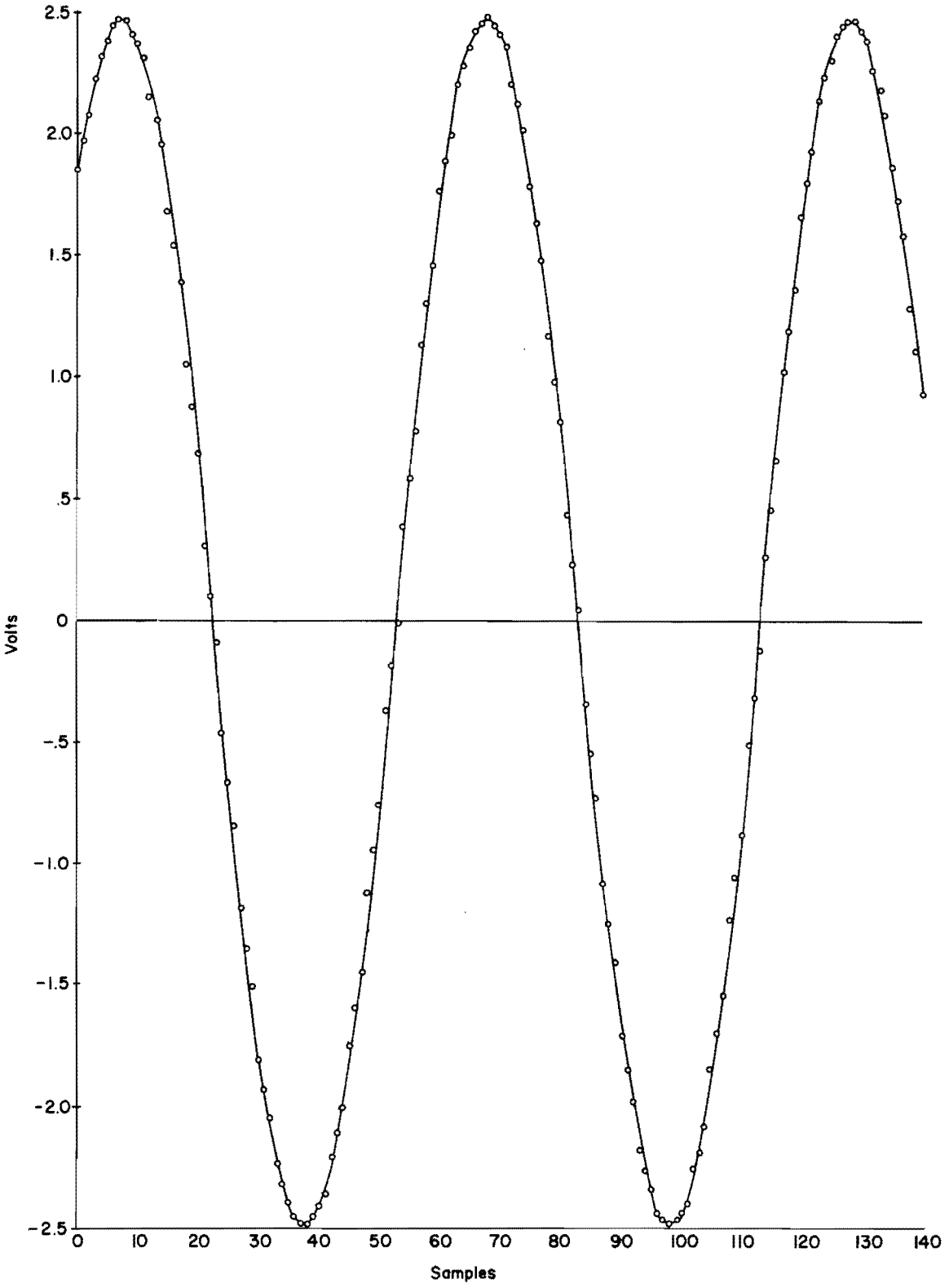

Fig 6.1. A-D test channels 0, 2, and 4.

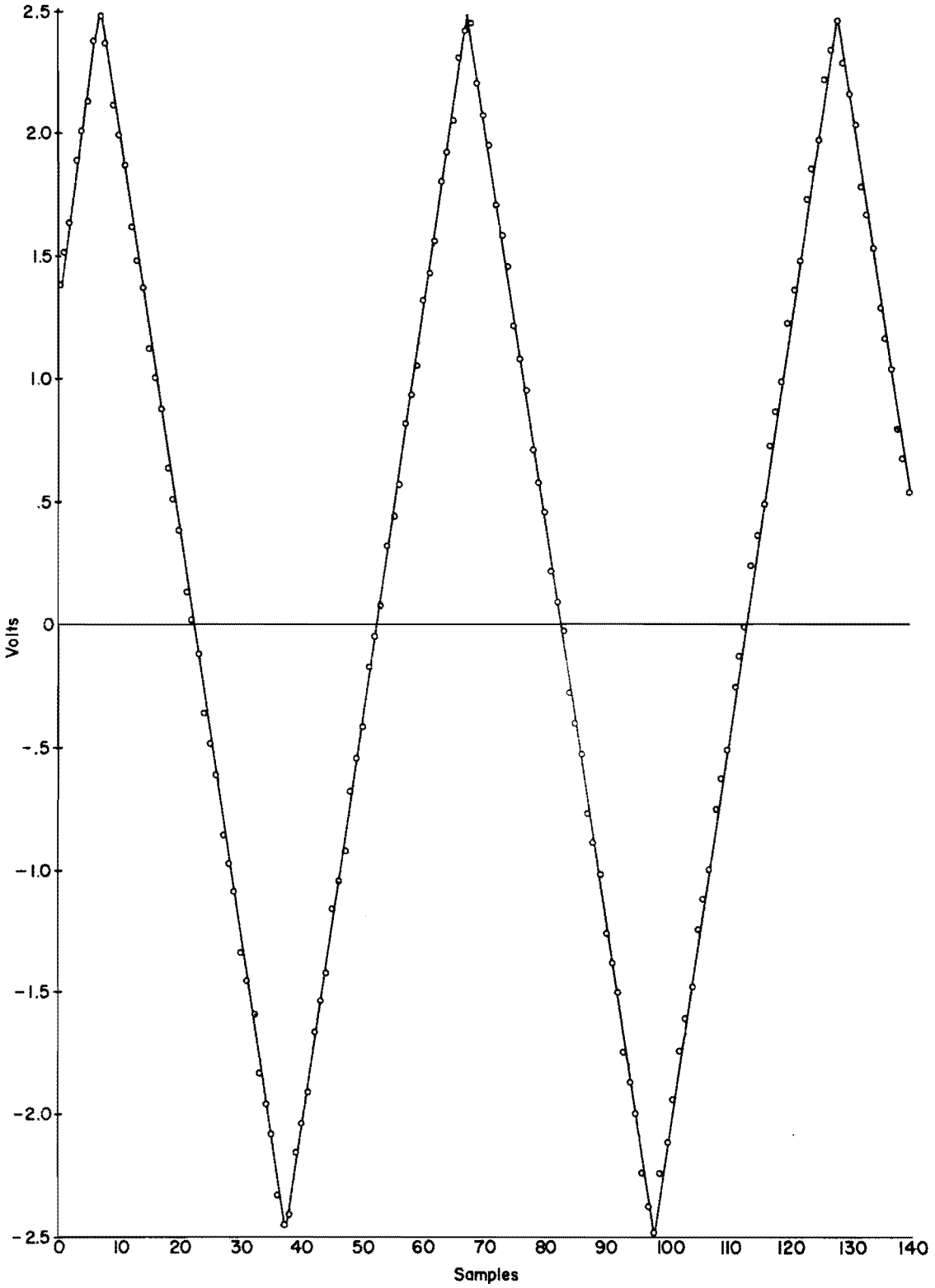

Fig 6.2. A-D test channels 1, 3, and 5.

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3. Technical Manual, Instructions for Honeywell Model 8100 Portable Recorder/ Reproducer, Honeywell-Test Instruments Division, Denver, Colorado, January 1966.

4. Operating and Service Manual Model 8003A Pulse Generator, Hewlett-Packard, Palo Alto, California, September 1968.

5. Manual for Interface Kit 12554A/M1/M1, M2/M1, M3 16-Bit Duplex Register for use with Raytheon Multiverter, Hewlett-Packard, Palo Alto, California, May 1968.

6. A Pocket Guide to Hewlett-Packard Computers, Hewlett-Packard, Palo Alto, California.

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APPENDICES

APPENDIX 1

SYSTEM CABLING INFORMATION

ANALOG IN

From Analog Recorder (Winchester)		To Interface (Blue Ribbon)	
Pin (J2)	Signal	Pin	Signal
C	Ground	13	Ground
A	Channel 1 data	1	Channel 1 data
F		14	
B	Channel 2 data	2	Channel 2 data
E		15	
D	Channel 3 data	3	Channel 3 data
K		16	
H	Channel 4 data	4	Channel 4 data
N		17	
J	Channel 5 data	5	Channel 5 data
M		18	
L	Channel 6 data	6	Channel 6 data
S		19	
P	Channel 7 data	7	Channel 7 data
V	Ground	20	Ground
R	Channel 8 data	8	Channel 8 data

ANALOG OUT

From Interface (Blue Ribbon)		To Multiverter (Plate)	
Pin	Signal	Pin (J46)	Signal
1	Channel 1 data	1	Channel 1 data
2	Channel 2 data	2	Channel 2 data
3	Channel 3 data	3	Channel 3 data
4	Channel 4 data	4	Channel 4 data
5	Channel 5 data	5	Channel 5 data
6	Channel 6 data	6	Channel 6 data
7	Channel 7 data	7	Channel 7 data
8	Channel 8 data	8	Channel 8 data

GATED INPUT SIGNAL

From Multiverter (Plate)		To Pulse Generator (BNC)	
Pin	Signal	Pin	Signal
J46A	Trigger	Trigger Input	Gated, -2 volts D.C. coupled

DUPLEX IN

From Duplex Register Card		To Duplex Line (Blue Ribbon)	
Pin	Signal	Pin	Signal
A	0	5	0
B	1	6	1
C	2	7	2
AA	Encode	8	Encode

TRIGGERED INPUT

From Interface (BNC)		To Pulse Generator (BNC)	
Pin	Signal	Pin	Signal
Channel 5	Pulse	Trigger input	Pulse

SAMPLING SIGNAL

From Pulse Generator (BNC)		To Multiverter (BNC)	
Pin	Signal	Pin	Signal
J45	Negative triggered sampling rate	-Output/50 Ω	Negative triggered output sampling rate

DUPLEX OUT

From Duplex Line (Blue Ribbon)		To Duplex Register Card	
Pin	Signal	Pin	Signal
1	0	1	0
2	1	2	1
3	Flag	3	2
4	2		
5			
6			
7			
8			
		23	Flag
Shield	Ground	24	Ground

HP 2115 I/O CHANNEL CONFIGURATION

	ADDR (base 8)	Channel Data
2020 magnetic tape controller	10	1
2020 magnetic tape timing (command channel)	11	2
16 bit duplex register (A/D) (negative)	12	3
High-speed paper tape reader	13	4
Teletype	14	5
9 channel magnetic tape (data channel)	15	6
9 channel magnetic tape (command channel)	16	7
16 bit duplex register (positive)	17	8

APPENDIX 2

DATA CONVERSION PROGRAM
LISTING, SAMP

```
 PAGE 0001

0001                          ASMB,R,B,L,T
C       R 000070
FIN     R 000225
MVC     R 000323
OUT     R 000006
T2      R 000237
WT2     R 000275
WT3     R 000303
WT4     R 000307
.3030   R 000223
.IOC.   X 000001
ADCW1   R 000212
ADCW2   R 000213
BUFIN   R 000216
BUFIO   R 000220
BUF2N   R 000217
BUF2O   R 000221
CHECK   R 000011
CLEAR   R 000224
CON4    R 000253
CONTI   R 000243
DIGIT   R 000047
DM1F    R 000203
DM2F    R 000172
DMA1F   R 000125
DMA2F   R 000206
DMAIN   R 000214
DMAOU   R 000215
DUPLE   R 000010
ERROR   R 000210
IBUF1   C 000010
IBUF2   C 002744
IDENT   C 000003
IREAD   C 000000
ISWS2   C 005700
ISWSC   C 000002
IWRIT   C 000001
SAMP    R 000024
SETLE   R 000016
SIZE    R 000222
STA12   R 000324
STALL   R 000325
STATU   R 000020
TEST    R 000041
TEST2   R 000251
WRB1    R 000262
WRB2    R 000270
XVII    R 000000
**   NO ERRORS*
```

```
 PAGE 0002 #01  BUFFER IN - BUFFER OUT     SERIES   2.0

0001                    ASMB,R,B,L,T
0003  00000                      NAM SMPLE
0004*                            SAMP
0005                             ENT SAMP
0006                             COM IREAD,IWRIT,ISWSC,IDENT(5),IBUF1(1500)
0007                             COM IBUF2(1500)
0008                            COM ISWS2
0009*
0010  00000 000000  XVII   NOP
0011  00001 102317         SFS 17B
0012  00002 026006R         JMP OUT
0013  00003 102517         LIA 17B
0014  00004 103717         STC 17B,C
0015  00005 072010R         STA DUPLE
0016  00006 062010R OUT    LDA DUPLE
0017  00007 126000R         JMP XVII,I
0018*
0019  00010 000000  DUPLE  OCT 0  DUPLEX REGISTER CONTENTS
0020*
0021  00011 000000  CHECK  NOP
0022  00012 016000R         JSB XVII
0023  00013 000010         SLA
0024  00014 126011R         JMP CHECK,I
0025  00015 026225R         JMP FIN
0026*
0027                         EXT .IOC.
0028*
0029                         ENT SETLE
0030  00016          SETLE  EQU *
0031  00016 000000         NOP
0032  00017 016001X         JSB .IOC.
0033  00020          STATU  EQU *
0034  00020 040000         OCT 040000
0035  00021 002020         SSA
0036  00022 026017R         JMP *-3
0037  00023 126016R         JMP SETLE,I
0038*
0039  00024 000000  SAMP   NOP
0040  00025 016016R         JSB SETLE
0041  00026 062324R         LDA STA12
0042  00027 072020R         STA STATU
0043  00030 103100         CLF 0          DISABLE INTERRUPT SYSTEM
0044  00031 006400         CLB            USE B REGISTER FOR ERROR COUNT
0045  00032 076004C         STB IDENT+1
0046  00033 076000C         STB IREAD
0047  00034 076001C         STB IWRIT
0048  00035 076010R         STB DUPLE     ENABLE DUPLEX REGISTER & CLEAR
0049  00036 103717         STC 17B,C     THE FLAG & PREVIOUS DUPLEX INPUT
0050  00037 062323R         LDA MVC
0051  00040 072005C         STA IDENT+2
0052*
0053  00041          TEST   EQU *
0054  00041 016000R         JSB XVII   AUTO-MAGIC MODE
0055  00042 002011         SLA,RSS
0056  00043 026041R         JMP TEST      IF ZERO, WAIT A LITTLE LONGER
0057  00044 001300         RAR
0058  00045 002011         SLA,RSS
0059  00046 026041R         JMP TEST     IF BOTH BITS #0 & #1 ARE SET,
```

```
PAGE 0003 #01  BUFFER IN - BUFFER OUT     SERIES   2.0

0060*                                        GO TO DIGIT
0061  00047          DIGIT EQU *
0062*                                  PREPARE DMA1 FOR INPUT TO IBUF1
0063  00047 062214R          LDA DMAIN
0064  00050 102606           OTA 6
0065  00051 106702           CLC 2
0066  00052 062216R          LDA BUF1N
0067  00053 102602           OTA 2
0068  00054 102702           STC 2
0069  00055 062222R          LDA SIZE
0070  00056 102602           OTA 2
0071*  INITIATE DMA1 INPUT TO IBUF1
0072  00057 062212R         LDA ADCW1
0073  00060 102612          OTA 12B
0074  00061 062213R         LDA ADCW2
0075  00062 102612          OTA 12B
0076  00063 103712          STC 12B,C
0077  00064 103706           STC 6,C       TURN ON DMA CHANNEL # 1
0078*  SET IREAD TO ZERO
0079  00065 002400           CLA
0080  00066 072000C          STA IREAD
0081  00067 016011R         JSB CHECK     MAYBE YOU COME BACK & MAYBE NOT
0082  00070           C      EQU *
0083*   PREPARE DMA2 FOR INPUT INTO IBUF2
0084  00070 062214R          LDA DMAIN
0085  00071 102607           OTA 7
0086  00072 106703           CLC 3
0087  00073 062217R          LDA BUF2N
0088  00074 102603           OTA 3
0089  00075 102703           STC 3
0090  00076 062222R          LDA SIZE
0091  00077 102603           OTA 3
0092*   HAS BUFFER #1 BEEN FILLED YET
0093  00100 102306           SFS 6
0094  00101 026100R          JMP *-1     WAIT UNTIL BUFFER 1 IS FILLED
0095*
0096*   INITIATE DMA2 INPUT TO BUFFER 2
0097  00102 103712          STC 12B,C
0098  00103 103707           STC 7,C
0099*  A
0100*   SET  IREAD TO 1    ( POINT A IN FLOW CHART )
0101  00104 002404           CLA,INA
0102  00105 072000C          STA IREAD
0103*                                  PREPARE DMA1 FOR OUTPUT FROM IBUF1
0104  00106 062215R          LDA DMAOU     PREPARE DMA1 FOR OUTPUT
0105  00107 102606           OTA 6
0106  00110 106702           CLC 2
0107  00111 062220R          LDA BUF1O
0108  00112 102602           OTA 2
0109  00113 102702           STC 2
0110  00114 062222R          LDA SIZE
0111  00115 102602           OTA 2
0112  00116 102316         SFS 16B   3030 READY ?  SKIP IF  YES
0113  00117 026116R         JMP *-1   JUMP TO *-1   IF   NOT READY
0114*   INITIATE OUTPUT VIA DMA1 FROM IBUF1
0115  00120 062223R         LDA .3030
0116  00121 103616          OTA 16B,C
0117  00122 103706          STC 6,C
```

```
 PAGE 0004 #01  BUFFER IN - BUFFER OUT     SERIES   2.0


0118*   SET IWRIT TO ZERO
0119  00123 002400          CLA
0120  00124 072001C         STA IWRIT
0121*   HAS DMA1 FINISHED OUTPUTTING
0122  00125           DMA1F EQU *
0123  00125 102306          SFS 6
0124  00126 026206R         JMP DMA2F
0125  00127 036004C         ISZ IDENT+1  INCREMENT RECORD COUNT
0126  00130 102516         LIA 16B
0127  00131 001300         RAR        CHECH FOR & COUNT ERRORS ON 3030
0128  00132 000010         SLA
0129  00133 034001         ISZ 1           B REGISTER FOR ERROR COUNT
0130  00134 016011R        JSB CHECK     MAYBE YOU COME BACK & MAYBE NOT
0131  00135 062214R         LDA DMAIN
0132  00136 102606          OTA 6
0133  00137 106702          CLC 2
0134  00140 062216R         LDA BUF1N
0135  00141 102602          OTA 2
0136  00142 102702          STC 2
0137  00143 062222R         LDA SIZE
0138  00144 102602          OTA 2
0139*   HAS DMA2 FINISHED INPUTING
0140  00145 102307          SFS 7
0141  00146 026145R         JMP *-1
0142*                      INITIATE DMA1 INPUT TO BUFFER 1
0143  00147 103712         STC 12B,C
0144  00150 103706         STC 6,C
0145*                      SET IREAD TO ZERO TO DESIGNATE
0146*                      IBUF1 AS A READ AREA
0147  00151 002400         CLA
0148  00152 072000C        STA IREAD
0149*                                PREPARE DMA2 FOR OUTPUT FROM IBUF2
0150  00153 062215R         LDA DMAOU
0151  00154 102607          OTA 7
0152  00155 106703          CLC 3
0153  00156 062221R         LDA BUF2O
0154  00157 102603          OTA 3
0155  00160 102703          STC 3
0156  00161 062222R         LDA SIZE
0157  00162 102603         OTA 3
0158  00163 102316         SFS 16B
0159  00164 026163R        JMP *-1
0160  00165 062223R        LDA .3030      START THE 3030
0161  00166 103616         OTA 16B,C      COMMAND CHANNEL IS 16 OCTAL
0162*  INITIATE OUTPUT VIA DMA2 FROM IBUF2
0163  00167 103707          STC 7,C       DMA
0164*  SET WRITE = 1
0165  00170 002404          CLA,INA
0166  00171 072001C         STA IWRIT
0167*  DMA2 FINISHED
0168  00172           DM2F  EQU *
0169  00172 102307          SFS 7
0170  00173 026203R         JMP DM1F  CHECK TO SEE IF INPUT FINISHED FIRS
0171  00174 036004C         ISZ IDENT+1  INCREMENT RECORD COUNT
0172  00175 102516         LIA 16B  CHECK FOR & COUNT ERRORS ON 3030
0173  00176 001300         RAR
0174  00177 000010         SLA
0175  00200 034001         ISZ 1          B REGISTER FOR ERROR COUNT
```

```
PAGE 0005 #01  BUFFER IN - BUFFER OUT     SERIES   2.0

0176  00201 016011R        JSB CHECK     MAYBE YOU COME BACK & MAYBE NOT
0177  00202 026070R         JMP C
0178  00203          DM1F   EQU *
0179  00203 102306          SFS 6
0180  00204 026172R         JMP DM2F
0181  00205 026210R         JMP ERROR  IF A/D INPUT FINISHED FIRST, GO TO
0182  00206 102307  DMA2F SFS 7     HAS DMA2 INPUTTING FINISHED FIRST?
0183  00207 026125R        JMP DMA1F
0184  00210          ERROR EQU *
0185  00210 102011         HLT 11B
0186  00211 026225R        JMP FIN
0187  00212 000000   ADCW1 OCT 0
0188  00213 140000   ADCW2 OCT 140000
0189  00214 120012   DMAIN OCT 120012
0190  00215 160015   DMAOU OCT 160015
0191  00216 100010C BUF1N DEF IBUF1,I
0192  00217 102744C BUF2N DEF IBUF2,I
0193  00220 000010C BUF1O DEF IBUF1
0194  00221 002744C BUF2O DEF IBUF2
0195  00222 175044   SIZE  DEC -1500
0196  00223 000031   .3030 OCT 31       3030 CONTROL WORD ( S )
0197  00224 000300   CLEAR OCT 300
0198*
0199  00225          FIN   EQU *
0200  00225 107717         CLC 17B,C
0201  00226 036004C        ISZ IDENT+1
0202  00227 062000C         LDA IREAD  DISCONNECT READ CH
0203  00230 002002          SZA
0204  00231 026237R        JMP T2
0205  00232 102306         SFS 6
0206  00233 026232R        JMP *-1
0207  00234 106706         CLC 6
0208  00235 106712         CLC 12B
0209  00236 026243R        JMP CONTI
0210*
0211  00237          T2    EQU *
0212  00237 102307         SFS 7
0213  00240 026237R        JMP *-1
0214  00241 106707         CLC 7
0215  00242 106712         CLC 12B
0216*
0217  00243          CONTI EQU *
0218  00243 062001C         LDA IWRIT   WAIT UNTIL WRITE COMPLETE
0219  00244 002002          SZA
0220  00245 026251R        JMP TEST2
0221  00246 102306         SFS 6          TEST DMA1 FOR COMPLETION
0222  00247 026246R         JMP *-1
0223  00250 026253R         JMP CON4
0224  00251 102307  TEST2  SFS 7        TEST DMA2
0225  00252 026251R         JMP *-1
0226  00253          CON4   EQU *
0227  00253 102316         SFS 16B
0228  00254 026253R        JMP *-1
0229*                     STOP THE 30 30 TAPE UNIT!
0230  00255 106700         CLC 0
0231  00256 016016R        JSB SETLE
0232  00257 062000C        LDA IREAD  WRITE LAST BUFFER
0233*
```

```
 PAGE 0006 #01  BUFFER IN - BUFFER OUT     SERIES   2.0


0234*
0235   00260 002002          SZA
0236   00261 026270R         JMP WRB2
0237   00262 016001X WRB1    JSB .IOC.    WRITE BUF1
0238   00263 020112          OCT 20112
0239   00264 026262R         JMP WRB1
0240   00265 000010C         DEF IBUF1
0241   00266 002734          DEC 1500
0242   00267 026275R         JMP WT2
0243   00270 016001X WRB2    JSB .IOC.    WRITE BUF2
0244   00271 020112          OCT 20112
0245   00272 026270R         JMP WRB2
0246   00273 002744C         DEF IBUF2
0247   00274 002734          DEC 1500
0248   00275           WT2   EQU *
0249   00275 016016R         JSB SETLE
0250   00276 016001X         JSB .IOC.     WRITE IDENT
0251   00277 020112          OCT 20112
0252   00300 026275R         JMP WT2
0253   00301 000003C         DEF IDENT
0254   00302 000006          DEC 6
0255   00303           WT3   EQU *
0256   00303 016016R         JSB SETLE
0257   00304 016001X         JSB .IOC.        WRITE EIND OF FILE
0258   00305 030112          OCT 30112
0259   00306 026303R         JMP WT3
0260   00307           WT4   EQU *
0261   00307 016016R         JSB SETLE
0262   00310 016001X         JSB .IOC.        WRITE END OF FILE
0263   00311 030112          OCT 30112
0264   00312 026307R         JMP WT4
0265   00313 016016R         JSB SETLE
0266   00314 016001X         JSB .IOC.     BACKSPACE THE 3030
0267   00315 030212          OCT 30212
0268   00316 026314R         JMP *-2
0269   00317 016016R         JSB SETLE
0270   00320 062325R         LDA STALL
0271   00321 072020R         STA STATU
0272   00322 126024R         JMP SAMP,I
0273*
0274   00323 002734  MVC     DEC 1500
0275   00324 040012  STAI2   OCT 040012
0276   00325 040000  STALL   OCT 040000 STATUS SYSTEM WORD
0277                         END
**   NO ERRORS*
```

```
 PAGE 0001

0001                        ASMB,R,B,L,I
.10    R 000027
.20    R 000033
.30    R 000015
.40    R 000042
.50    R 000023
.60    R 000060
.70    R 000036
.90    R 000050
BSK    R 000144
LOC    R 000142
STS    R 000152
.110   R 000065
.120   R 000102
.130   R 000075
.140   R 000107
.141   R 000110
.150   R 000123
.180   R 000131
.ENTR  X 000001
.IOC.  X 000002
AGMTS  R 000000
EXIT   R 000134
FILOC  R 000002
FWONE  R 000165
IDENT  C 000003
IDUM   C 000000
NFILE  R 000141
RDIDT  R 000173
REWD   R 000215
TEMP   R 000143
**   NO ERRORS*
```

PAGE 0002 #01

```
0001                    ASMB,R,B,L,T
0002  00000                     NAM FILOC
0003                            COM IDUM(3),IDENT(5)
0004                            ENT FILOC
0005                            EXT .ENTR
0006                            EXT .IOC.
0007  00000 000000  AGMTS BSS 2
0008  00002 000000  FILOC NOP
0009  00003 016001X        JSB .ENTR
0010  00004 000000R        DEF AGMTS
0011  00005 162000R        LDA AGMTS,I
0012  00006 072141R        STA NFILE
0013  00007 162001R        LDA AGMTS+1,I
0014  00010 072142R        STA LOC
0015* TEST LOC STATUS(TAPE POSITIONING)
0016  00011 002003         SZA,RSS
0017  00012 026033R        JMP .20     LOC=0
0018  00013 002020         SSA
0019  00014 026027R        JMP .10     LOC=-1
0020  00015 062141R .30    LDA NFILE   LOC=+1 ,CHECK NFILE
0021  00016 002003         SZA,RSS
0022  00017 026023R        JMP .50     NFILE=0
0023  00020 002020         SSA
0024  00021 026042R        JMP .40     NFILE =-1
0025  00022 026060R        JMP .60     NFILE =+1
0026  00023 016215R .50    JSB REWD    REWIND AND WRITE EOF
0027  00024 002404         CLA,INA
0028  00025 072142R        STA LOC     SET LOC=1
0029  00026 026134R         JMP EXIT
0030  00027 016144R .10    JSB BSK    BACKSPACE 1 RECORD
0031  00030 002404         CLA,INA
0032  00031 072142R        STA LOC    SET LOC=1
0033  00032 026015R        JMP .30
0034  00033 062141R .20    LDA NFILE
0035  00034 002003         SZA,RSS
0036  00035 026015R         JMP .30
0037  00036 016165R .70    JSB FWONE   SKIP ONE RECORD
0038  00037 002404         CLA,INA
0039  00040 072142R        STA LOC    SET LOC=1
0040  00041 026015R        JMP .30
0041  00042 016165R .40    JSB FWONE
0042  00043 002003         SZA,RSS     NOT EOF
0043  00044 026042R        JMP .40
0044  00045 016165R        JSB FWONE
0045  00046 002003         SZA,RSS
0046  00047 026042R        JMP .40     NOT EOF
0047  00050 016144R .90    JSB BSK
0048  00051 016144R        JSB BSK
0049  00052 016144R        JSB BSK
0050  00053 016173R        JSB RDIDT   READ IDENT
0051  00054 016165R        JSB FWONE
0052  00055 002404         CLA,INA
0053  00056 072142R        STA LOC     SET LOC=1
0054  00057 026134R         JMP EXIT
0055  00060 016165R .60    JSB FWONE    A=1=EOF
0056  00061 002003         SZA,RSS
0057  00062 026060R        JMP .60     NOT EOF
0058  00063 016144R        JSB BSK
```

```
PAGE 0003 #01


0059  00064 016144R        JSB BSK
0060  00065 016173R .110   JSB  RDIDT
0061  00066 062003C        LDA IDENT
0062  00067 003004         CMA,INA
0063  00070 042141R        ADA NFILE
0064  00071 002003         SZA,RSS  CHECK FOR ZERO
0065  00072 026102R        JMP .120  ZERO
0066  00073 002021         SSA,RSS
0067  00074 026107R        JMP .140  POSITIVE
0068  00075 016144R .130   JSB  BSK   NEGATIVE
0069  00076 002003         SZA,RSS
0070  00077 026075R        JMP .130   NOT EOF
0071  00100 016144R        JSB BSK
0072  00101 026065R        JMP .110
0073  00102 016144R .120   JSB BSK
0074  00103 002003         SZA,RSS
0075  00104 026102R        JMP .120   NOT EOF
0076  00105 016165R        JSB FWONE
0077* LEAVE TAPE AT BEGINNING OF FILE
0078* LOCATED BY THIS ROUTINE
0079  00106 026134R         JMP EXIT
0080  00107 016165R .140   JSB FWONE
0081  00110 016165R .141   JSB FWONE
0082  00111 002003         SZA,RSS
0083  00112 026110R        JMP .141   NOT EOF
0084  00113 016165R        JSB FWONE
0085  00114 072143R        STA TEMP
0086  00115 016144R        JSB BSK        2ND EOF
0087  00116 016144R        JSB BSK        1ST EOF
0088  00117 016144R        JSB BSK        IDENT
0089  00120 062143R        LDA TEMP
0090  00121 002003         SZA,RSS
0091  00122 026065R        JMP .110  NOT EOF
0092  00123 016173R .150   JSB RDIDT  READ IDENT
0093  00124 062003C        LDA IDENT
0094  00125 003004         CMA,INA
0095  00126 042141R        ADA NFILE
0096  00127 002003         SZA,RSS
0097  00130 026102R        JMP .120  ZERO EQUAL
0098  00131 062141R .180   LDA NFILE NOT EQUAL
0099  00132 006404         CLB,INB   B=1 INDICATES FILE NOT
0100*                     ON DATA TAPE
0101  00133 102000         HLT
0102  00134 066142R EXIT   LDB LOC
0103  00135 176001R        STB AGMTS+1,I
0104  00136 066141R        LDB NFILE
0105  00137 176000R        STB AGMTS,I
0106  00140 126002R        JMP FILOC,I
0107  00141 000000  NFILE  BSS 1
0108  00142 000000  LOC    BSS 1
0109  00143 000000  TEMP   OCT 0
0110  00144 000000  BSK    NOP           BSK BACK SPACES ONE RECORD
0111  00145 016002X        JSB .IOC.
0112  00146 030212         OCT 030212      BACKSPACE
0113  00147 026145R        JMP *-2
0114  00150 016152R        JSB STS
0115  00151 126144R        JMP BSK,I
0116  00152 000000  STS    NOP           STS OBTAINS EOF INFORMATION
```

PAGE 0004 #01

```
0117  00153 016002X        JSB .IOC.
0118  00154 040012         OCT 040012
0119  00155 002020         SSA
0120  00156 026153R        JMP *-3
0121  00157 001323         RAR,RAR
0122  00160 001323         RAR,RAR
0123  00161 001323         RAR,RAR
0124  00162 001300         RAR
0125  00163 012226R        AND =B1
0126  00164 126152R        JMP STS,I
0127  00165 000000  FWONE  NOP              FWONE SPACES FORWARD 1 REC
0128  00166 016002X        JSB .IOC.
0129  00167 030312         OCT 030312
0130  00170 026166R        JMP *-2
0131  00171 016152R        JSB STS
0132  00172 126165R        JMP FWONE,I
0133  00173 000000  RDIDT  NOP
0134  00174 016002X        JSB .IOC.
0135  00175 010112         OCT 010112
0136  00176 026174R        JMP *-2
0137  00177 000003C        DEF IDENT
0138  00200 000005         DEC 5
0139  00201 016002X        JSB .IOC.
0140  00202 040012         OCT 040012
0141  00203 002020         SSA
0142  00204 026201R        JMP *-3
0143  00205 012227R        AND =B22       CHECK FOR ERROR
0144  00206 002003         SZA,RSS
0145  00207 126173R        JMP RDIDT,I    READ OK
0146  00210 006404         CLB,INB
0147  00211 006004         INB       B=2 INDICATES READ ERROR
0148  00212 102000         HLT
0149  00213 016144R        JSB BSK  TRY AGAIN
0150  00214 026174R        JMP RDIDT+1
0151  00215 000000  REWD   NOP   REWD REWINDS AND WRITES EOF
0152  00216 016002X        JSB .IOC.
0153  00217 030412         OCT 030412
0154  00220 026216R        JMP *-2
0155  00221 016152R        JSB STS
0156  00222 016002X        JSB .IOC.
0157  00223 030112         OCT 030112     WRITE EOF
0158  00224 026222R        JMP *-2
0159  00225 126215R        JMP REWD,I
      00226 000001
      00227 000022
0160                       END
**   NO ERRORS*
```

```
FTN,B,L
      PROGRAM RWALK
C   A-D PROGRAM  SERIES 2.0  24 JAN 69
C   PART I
      COMMON  IREAD,IWRIT,ISWSC,IDENT(5),
     1  IBUF1(1500),IBUF2(1500)
C     SS2=1, AUTOMODE MODE
C     SS3=1, INHIBIT LIST OUT
C      CLEAR COMMON AREA
       DO 10 II=1,3005
 10    IDENT(II)= 0
 206   LOC = 0
C     CHECK FOR AUTOMODE
81     IF(ISSW(2))42,207
42     NFILE=-1
       GO TO 212
  207   WRITE (2,104)
  104 FORMAT ("ENTER FILE NUMBER")
      IERR = 0
      READ (1,*) NFILE,IERR
      IF (IERR) 207 , 212 , 207
C     CALL FILOC TO POSITION FILE FOR A-D
 212   CALL FILOC ( NFILE,LOC)
       IF(ISSW(3))31,32
32     CONTINUE
       WRITE (2, 106) ( IDENT (I),I=1,5)
  106 FORMAT (" FN = ",I5, "  NR = ",I5,"  NCLR = ",I5,
     1"  TAG ",I5, 2X , I5 )
31     IF(ISSW(2))43,75
43     IDENT(1)=IDENT(1)+1
       GO TO 220
   75 CONTINUE
      WRITE ( 2 , 108 )
  108 FORMAT (//" ENTER NEW FILE NUMBER AND TAG")
      IERR = 0
      READ (1,*) IDENT(1),IDENT(4),IDENT(5),IERR
      IF ( IERR ) 75,220,75
 220   CALL  SAMP
C      SAMP IS BUFFER IN/BUFFER OUT ROUTINE
      LOC = -1
       IF(ISSW(3))81,79
79     CONTINUE
C      PRINT IDENT OF LAST FILE WRITTEN
       WRITE (2,106) (IDENT(I),I=1,5)
       GO TO 81
       END
```

```
SMPLE

 02000 02325

LOAD

RWALK

 02326 02724

LOAD

FILOC

 02725 03154

LOAD

FRMTR

 03155 05230

 00241 00742

MPY

 05231 05341

FLOAT

 05342 05346

.PACK

 05347 05453

.ENTR

 05454 05521

DLDST
```

```
 05522 05557

IFIX

 00743 00777

.STOP

 05560 05600

.FLUN

 01000 01012

ISSW

 01013 01022

CLRIO

 05601 05605


*LST
.IOC.  13544
.SQT.  13515
.MEM.  13510
.BUFR  13712
SAMP   02024
SETLE  02016
RWALK  02331
CLRIO  05601
ISSW   01013
.DIO.  04632
.DTA.  04730
.IOI.  04527
FILOC  02727
.STOP  05560
.ENTR  05454
.BIO.  04705
.IOR.  04502
.IAR.  04566
.RAR.  04542
.FLUN  01000
.PACK  05347
FLOAT  05342
IFIX   00743
.MPY   05231
.DLD   05522
.DST   05532


*COM
 05606 13506
```

```
*LINKS
 01732 01777

*RUN
```

APPENDIX 3

TAPE WRITE PROGRAM
LISTING, SERVICE

```
FTN,B,L
      PROGRAM SERV
      DIMENSION DUM(8)
      COMMON IBUF(1500),IBEC,IDENT(5)
      IBEC=0
1     WRITE(2,100)
100    FORMAT("BEGIN DATA SERVICE ROUTINE")
      WRITE(2,500)
500   FORMAT("SET SS 10 FOR SS LIST")
      PAUSE 2
      IF(ISSW(10))501,502
501   WRITE(2,503)
503   FORMAT("SS 0  END SERVICE OPERATION"/,
     1"SS 1  USED TO SKIP THRU RECORDS (WORDS)"/,
     2"SS 2  USED FOR AUTOMATIC MODE"/,
     3"SS 3  USED TO SKIP THRU FILE (RECORDS)"/,
     4"SS 4  USED TO SKIP THRU DATA TAPE"/,
     5"SS 10 PROVIDES THIS INSTRUCTION LIST")
      WRITE(2,508)
508    FORMAT("SS 6 USED TO WRITE EOF")
      WRITE(2,504)
504   FORMAT("SS 13 USED TO LIST DATA"/,
     1"SS 14 USED TO WRITE 9 TO 7 TRACK TAPE"/,
     2"SS 15 USED TO LIST IDENTS")
502    CONTINUE
      PAUSE 1
      IF(ISSW(6))331,332
331   WRITE(2,335)
335   FORMAT("PUSH RUN TO WRITE EOF")
      PAUSE
      ENDFILE 7
      GO TO 1
332   CONTINUE
      IFLAG=1
29    IRR=0
      WRITE(2,101)
101   FORMAT("ENTER FILE NUMBER")
      READ(1,*)IIF,IRR
      IF(IRR)29,77,29
77    CONTINUE
      IFN=IIF
30    IF(IIF)3,3,2
3     CALL FILOC(1,IS)
      CALL FILOC(1,IS)
      IF(IS)130,4,26
4     CALL FILOC(1,IS)
      IF(IS)130,4,5
5     CALL FILOC(-1,IS)
      CALL FILOC(-1,IS)
      CALL RED30(IDENT,5)
      GO TO 6
2     CALL FILOC(1,IS)
7     CALL FILOC(1,IS)
      IF(IS)130,7,8
8     CALL FILOC(-1,IS)
9     CALL FILOC(-1,IS)
      CALL RED30(IDENT,5)
      IF(IFN-IDENT(1))10,6,11
10    CALL FILOC(-1,IS)
```

```
      IF(IS)130,10,9
11    CALL FILOC(1,IS)
12    CALL FILOC(1,IS)
      IF(IS)130,7,26
6     WRITE(2,102)IDENT
102   FORMAT(" FN= ",I5," NR= ",I5," NCLR= ",I5,
     1" TAGS ",I5,2X,I5,//)
104   FORMAT("END OF DATA")
      IF(ISSW(15))21,22
22    IF(ISSW(14))23,24
24    IF(ISSW(13))25,1
21    IF(ISSW(0))26,27
26    IF(IBEC)311,310,311
311   WRITE(2,317)IBEC
317   FORMAT(I5,"ERROR(S) ON 2020")
      IBEC=0
310   WRITE(2,104)
      IF(ISSW(14))28,1
28    ENDFILE 7
      GO TO 1
27    IF(ISSW(2))280,29
280   IFN=IFN+1
      GO TO 3
23    GO TO (31,32)IFLAG
31    IFLAG=2
      ENDFILE 7
107   IERR =0
      WRITE(2,106)
106   FORMAT("ENTER 1,0 FOR 10,5 VOLT RESOLUTION")
      READ(1,*)IRS,IERR
      IF(IERR)107,32,107
32    K=IDENT(2)+1
      DO 33 I=1,K
33    CALL FILOC(-1,IS)
      KK=IDENT(2)
      DO 34 I=1,KK
      CALL RED30(IBUF,1500)
34    CALL WRT7(-1500,IRS)
      J=1
      DO 35 I=1,5
      IBUF(J)=0
      IBUF(J+1)=IDENT(I)*(-1)
35    J=J+2
      CALL WRT7(-10,0)
      ENDFILE 7
      CALL FILOC(1,IS)
      GO TO 21
25    GO TO (41,42)IFLAG
41    IFLAG=2
109   IERR =0
      WRITE(2,111)
111   FORMAT("ENTER NO OF CHANNELS")
      READ(1,*)NC,IERR
      IF(IERR)109,42,109
42    K=IDENT(2)+1
      DO 420 I=1,K
420   CALL FILOC(-1,IS)
```

```
      K=IDENT(2)
      DO 44 I=1,K
51    CALL RED3Ø(IBUF,15ØØ)
      DO 73 J=1,15ØØ,NC
      L=J
      DO 185 IRO=1,NC
      DUM(IRO)=FLOAT(IBUF(L))*(5./2Ø48.)*(-1.)
185   L=L+1
      IF(ISSW(1))73Ø,46
73Ø    DO 731 IRO=1,1ØØØØ
731   CONTINUE
      GO TO 73
46    WRITE(2,112)I,J,(DUM(KL),KL=1,NC)
112   FORMAT(2I4,8(XF7.3))
      IF(ISSW(4))47,686
686   IF(ISSW(3))44,48
48    IF(ISSW(Ø))47,73
47    CALL FILOC(1,IS)
      IF(IS)4Ø1,47,4Ø1
4Ø1   CALL FILOC(-1,IS)
      GO TO 21
73    CONTINUE
44    CONTINUE
      CALL FILOC(1,IS)
      GO TO 47
52    CALL FILOC(-1,IS)
      GO TO 27
13Ø   PAUSE
      GO TO 1
      END
      END$
```

```
 PAGE 0001

0001                    ASMB,R,B,L,T
B       R 000016
BSK     R 000024
LOC     R 000022
STS     R 000032
.ENTR   X 000001
.IOC.   X 000002
AGMTS   R 000000
EXIT    R 000017
FILOC   R 000002
FWONE   R 000045
NFILE   R 000021
TEMP    R 000023
**   NO ERRORS*
```

```
PAGE 0002 #01

0001                    ASMB,R,B,L,T
0002  00000                     NAM FILOC
0003                            ENT FILOC
0004                            EXT .ENTR
0005                            EXT .IOC.
0006  00000 000000  AGMTS BSS 2
0007  00002 000000  FILOC NOP
0008  00003 016001X       JSB .ENTR
0009  00004 000000R       DEF AGMTS
0010  00005 162000R       LDA AGMTS,I
0011  00006 072021R       STA NFILE
0012  00007 162001R       LDA AGMTS+1,I
0013  00010 072022R       STA LOC
0014* TEST LOC STATUS(TAPE POSITIONING)
0015  00011 062021R        LDA NFILE
0016  00012 002020        SSA
0017  00013 026016R       JMP B
0018  00014 016045R       JSB FWONE
0019  00015 026017R       JMP EXIT
0020  00016 016024R B     JSB BSK
0021  00017 172001R EXIT  STA AGMTS+1,I
0022  00020 126002R       JMP FILOC,I
0023  00021 000000  NFILE BSS 1
0024  00022 000000  LOC   BSS 1
0025  00023 000000  TEMP  OCT 0
0026  00024 000000  BSK   NOP             BSK BACK SPACES ONE RECORD
0027  00025 016002X       JSB .IOC.
0028  00026 030212        OCT 030212        BACKSPACE
0029  00027 026025R       JMP *-2
0030  00030 016032R       JSB STS
0031  00031 126024R       JMP BSK,I
0032  00032 000000  STS   NOP             STS OBTAINS EOF INFORMATION
0033  00033 016002X       JSB .IOC.
0034  00034 040012        OCT 040012
0035  00035 002020        SSA
0036  00036 026033R       JMP *-3
0037  00037 001323        RAR,RAR
0038  00040 001323        RAR,RAR
0039  00041 001323        RAR,RAR
0040  00042 001300        RAR
0041  00043 012053R       AND =B1
0042  00044 126032R       JMP STS,I
0043  00045 000000  FWONE NOP              FWONE SPACES FORWARD 1 REC
0044  00046 016002X       JSB .IOC.
0045  00047 030312        OCT 030312
0046  00050 026046R       JMP *-2
0047  00051 016032R       JSB STS
0048  00052 126045R       JMP FWONE,I
      00053 000001
0049                        END
**   NO ERRORS*
```

```
 PAGE 0001

0001                    ASMB,R,B,L
**   NO ERRORS*
```

```
 PAGE 0002 #01

0001                    ASMB,R,B,L
0002   00000                    NAM RED30
0003                            ENT RED30
0004                            EXT .ENTR,.IOC.
0005   00000 000000   IBUF1     NOP
0006   00001 000000   CT        NOP
0007   00002 000000   RED30     NOP
0008   00003 016001X            JSB .ENTR
0009   00004 000000R            DEF IBUF1
0010   00005 000001R            DEF CT
0011   00006 016002X            JSB .IOC.  CHECK FOR BUSY OR LOCAL
0012   00007 040012             OCT 040012
0013   00010 000010             SLA
0014   00011 102024             HLT 24B
0015   00012 062000R            LDA IBUF1
0016   00013 072021R            STA *+6
0017   00014 162001R            LDA CT,I
0018   00015 072022R            STA *+5
0019   00016 016002X            JSB .IOC.
0020   00017 010112             OCT 010112
0021   00020 026016R            JMP *-2
0022   00021 000000             DEF 0
0023   00022 000000             DEF 0
0024   00023 016002X            JSB .IOC.
0025   00024 040012             OCT 040012
0026   00025 002020             SSA
0027   00026 026023R            JMP *-3
0028   00027 001200             RAL
0029   00030 002020             SSA
0030   00031 102025             HLT 25B  TRANSMISSION ERROR OR LOCAL
0031   00032 012036R            AND MASK1
0032   00033 002002             SZA
0033   00034 102026             HLT 26B
0034   00035 126002R            JMP RED30,I
0035   00036 000400   MASK1     OCT 400
0036                            END
**   NO ERRORS*
```

```
 PAGE 0001

0001                    ASMB,R,B,L
**   NO ERRORS*
```

PAGE 0002 #01

```
0001                    ASMB,R,B,L
0002  00000                     NAM WRT7
0003                            COM IBUF(1500)
0004                            ENT WRT7
0005                            EXT .IOC.
0006                            EXT .ENTR
0007  00000 000000  .1500 NOP
0008  00001 000000  IRS   BSS 1
0009  00002 000000  WRT7  NOP
0010  00003 016002X       JSB .ENTR
0011  00004 000000R       DEF .1500
0012  00005 000001R       DEF IRS
0013  00006 016001X       JSB .IOC.
0014  00007 040000        OCT 040000
0015  00010 002020        SSA
0016  00011 026006R       JMP *-3
0017  00012 062075R LP5   LDA TEM2
0018  00013 072100R       STA TEM1
0019  00014 162000R       LDA .1500,I
0020  00015 072074R       STA CT
0021  00016 062072R       LDA .17
0022  00017 102611        OTA 11B
0023  00020 162100R LOOP  LDA TEM1,I
0024  00021 003004        CMA,INA
0025  00022 166001R       LDB IRS,I
0026  00023 004010        SLB
0027  00024 001100        ARS
0028  00025 072077R       STA FROG
0029  00026 001121        ARS,ARS
0030  00027 001121        ARS,ARS
0031  00030 001121        ARS,ARS
0032  00031 102310        SFS 10B
0033  00032 026031R       JMP *-1
0034  00033 103610        OTA 10B,C
0035  00034 062077R       LDA FROG
0036  00035 102310        SFS 10B
0037  00036 026035R       JMP *-1
0038  00037 103610        OTA 10B,C
0039  00040 036074R       ISZ CT
0040  00041 026043R       JMP *+2
0041  00042 026047R       JMP EXIT
0042  00043 062100R       LDA TEM1
0043  00044 042073R       ADA ONE
0044  00045 072100R       STA TEM1
0045  00046 026020R       JMP LOOP
0046  00047 106710  EXIT  CLC 10B
0047  00050 002400        CLA
0048  00051 102611        OTA 11B
0049  00052 102311        SFS 11B
0050  00053 026052R       JMP *-1 CONTROLLER BUSY
0051  00054 102511        LIA 11B
0052  00055 001100        ARS
0053  00056 000010        SLA
0054  00057 026061R       JMP PERR
0055  00060 126002R       JMP WRT7,I
0056  00061 062101R PERR  LDA =B101
0057  00062 102611        OTA 11B
0058  00063 102311        SFS 11B
```

```
 PAGE 0003 #01


0059   00064 026063R        JMP *-1
0060   00065 062102R        LDA =B15
0061   00066 102611         OTA 11B
0062   00067 102311         SFS 11B
0063   00070 026067R        JMP *-1
0064   00071 026012R        JMP LP5
0065   00072 000071   .17   OCT 71
0066   00073 000001   ONE    OCT 1
0067   00074 000000   CT     BSS 1
0068   00075 000000C  TEM2   DEF IBUF
0069   00076 000000   PCK    BSS 1
0070   00077 000000   FROG   BSS 1
0071   00100 000000   TEM1   BSS 1
       00101 000101
       00102 000015
0072                         END
**   NO ERRORS*
```

```
SERV

 02000 04100

LOAD

WRT7

 04101 04206

LOAD

FILOC

 04207 04262

LOAD

RED30

 04263 04321

LOAD

FRMTR

 04322 06375

 00241 00742

..DLC

 06376 06407

FADSB

 06410 06553

FDV

 06554 06657
```

FMP

06660 06743

MPY

06744 07054

FLOAT

07055 07061

.PACK

07062 07166

DIV

07167 07261

.ENTR

07262 07327

DLDST

07330 07365

IFIX

07366 07422

.PAUS

07423 07444

.STOP

07445 07465

.GOTO

07466 07510

```
.FLUN

 07511 07523

ISSW

 07524 07533

.TAPE

 07534 07541

CLRIO

 07542 07546
.IOC.  13544
.SQI.  13515
.MEM.  13510
.BUFR  13712
SERV   02023
CLRIO  07542
.DIO.  05777
.DTA.  06075
.PAUS  07423
ISSW   07524
.TAPE  07534
.IOI.  05674
FILOC  04211
RED30  04265
.IAR.  05733
.GOTO  07466
WRT7   04103
.MPY   06744
FLOAT  07055
.DST   07340
.DLD   07330
.FDV   06554
.FMP   06660
..DLC  06376
.IOR.  05647
.STOP  07445
.ENTR  07262
.BIO.  06052
.RAR.  05707
.FLUN  07511
.PACK  07062
IFIX   07366
.FSB   06413
.FAD   06410
.DIV   07167

*COM
 10545 13506
```

```
*LST
.IOC.   13544
.SQT.   13515
.MEM.   13510
.BUFR   13712
SERV    02023
CLRIO   07542
.DIO.   05777
.DIA.   06075
.PAUS   07423
ISSW    07524
.TAPE   07534
.IOI.   05674
FILOC   04211
RED30   04265
.IAR.   05733
.GOTO   07466
WRT7    04103
.MPY    06744
FLOAT   07055
.DST    07340
.DLD    07330
.FDV    06554
.FMP    06660
..DLC   06376
.IOR.   05647
.STOP   07445
.ENTR   07262
.BIO.   06052
.RAR.   05707
.FLUN   07511
.PACK   07062
IFIX    07366
.FSB    06413
.FAD    06410
.DIV    07167

*COM
 10545 13506

*LINKS
 01653 01777

*END
```

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