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16. Abstract

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EVALUATION OF THE DATAMATE MODEL D-16

AS A TRAFFIC CONTROLLER

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Research Report 165-2

DEVELOPMENT OF URBAN TRAFFIC MANAGEMENT
AND CONTROL SYSTEMS

Research Study Number 2-18-72-165

Sponsored by
The Texas Highway Department
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TEXAS TRANSPORTATION INSTITUTE
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ABSTRACT

A minicomputer system has been installed as the centralized traffic data acquisition and freeway entrance ramp controller at the Gulf Freeway Surveillance and Control Center. This report documents and evaluates the minicomputer system development and operation after one year of freeway ramp control. Emphasis was directed toward the verification of the sensed and calculated freeway traffic data as well as providing programming and operational adjustments to reduce the effects of several deficiencies in the minicomputer system. Cost estimates and the level of effort expended for system implementation are given.

Key Words: Ramp Controller, Minicomputer, Operating Reliability, Traffic Control, Urban Freeways.

SUMMARY

Research Study Number 2-8-69-139, entitled "Freeway Control and Information Systems," conducted in 1968-71, had as one of its objectives the application of a small digital computer as the central controller for the Gulf Freeway Ramp Control System located in Houston, Texas. This report documents and evaluates the minicomputer development and operation after one year of freeway ramp control.

To aid in the development of specifications for the minicomputer system, a survey of the existing computer systems was conducted in 1970. It was determined that several systems (if modifications were provided) could satisfy the requirements of the ramp control application. The functional specifications were directed towards a minicomputer system that would best fit the application, without regards to specific marketed machines. This was accomplished so that the vendors would be able to respond to the fullest extent in their bidding presentations. Bids were received on seven minicomputer systems, none of which exactly satisfied the requirements of the specifications. Analysis of the bid responses resulted in the recommendation to accept the Datamate Model DM-16 Minicomputer system. This recommendation was based on the following results of the analysis of the bids: (1) the Datamate System contained the fewest critical alternatives to the specifications, (2) was the most cost effective of the acceptable systems, and (3) was the easiest to implement.

Initial startup problems with the traffic sensor input devices delayed the acceptance of the Datamate DM-16 minicomputer system. After redesigned input modules were installed, the DM-16 minicomputer completed the thirty-day acceptance

test. During the delay period, the computing system was utilized by project staff personnel for (1) familiarization with the system operations and (2) program development. Use of the computing system in an off-line mode presented an opportunity to review different aspects of the minicomputer system. This review process resulted in suggestions for specification changes and additions.

An operational evaluation of the Datamate DM-16 minicomputer as a freeway ramp controller was performed with two areas being closely investigated. The integrity of the sensed and calculated freeway traffic data was the primary investigated area. Results of tests indicated (1) speed measurements were within ± 1 mile per hour and (2) hourly flowrates were accurate to 3 vehicles per thousand as compared with the large research computer. The ability to retain this accuracy required total system reliability. Therefore, the second investigated area was concerned with discovering deficiencies which affected the ability of the DM-16 minicomputer to respond to the ramp control operation. Programming and operational adjustments were made to reduce the effects of several deficiencies that were identified.

The programs that enabled the Datamate DM-16 minicomputer to function as the central controller for the Gulf Freeway Ramp Control System covered three basic areas: operating system, ramp control, and system support. The operating system programs were unique to the application and the Datamate DM-16 minicomputer, but the logic of the remaining ramp control and system support programs were developed from previous work completed in the IBM Model 1800 digital computer. The level of effort and cost estimates for programming the Datamate Model DM-16

minicomputer are included.

Implementation

The role assumed by the Datamate Model DM-16 minicomputer in monitoring and controlling the freeway entrance ramp operation is the result of research previously conducted at the Gulf Freeway Surveillance Project. This report should clearly demonstrate the feasibility of utilizing a minicomputer as the central data acquisition and process controller.

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INTRODUCTION

The Texas Transportation Institute and the Texas Highway Department, in cooperation with the U.S. Department of Transportation, conducted the Research Study entitled "Freeway Control and Information Systems" on the Gulf Freeway in Houston, Texas during the period 1968-71. Two objectives of the research study; namely, (1) to develop and test a completely automatic freeway control system and (2) to provide technical assistance in the development of plans and specifications of other freeway control systems, were partially accomplished by the addition of a small central digital control computer. The procurement, testing, programming, operation, and evaluation of the small or minicomputer were under the direct supervision of the research project. The Research Study, "Development of Urban Traffic Management and Control Systems," is presently being conducted at the Houston facilities under the same operating agencies. An objective to be completed during the first year of this three-year study is an operational evaluation of the minicomputer as a ramp controller. This report presents the findings after one year of ramp control operations under minicomputer control.

The role of the minicomputer in monitoring and controlling the freeway ramp operations is the result of research previously conducted on the Gulf Freeway. Ramp control began in 1965 with the manual operation of the ramp signal indications by research personnel placed near each entrance ramp. After evaluation of two analog prototype controllers and manual metering operations, an eight-ramp analog control system was designed and implemented in 1967. The

analog control system is housed in the present Control Center and uses capacity-demand relationships to establish metering rates for the ramp signals. In order to provide the capability to research the gap acceptance or merging control theory and to apply system-wide interconnected control strategies to the ramp control system, a large research digital (IBM 1800 computer) was installed in 1968. During the 1968-71 study period, control programs were developed for the IBM Model 1800 digital computer, which then became the central ramp controller. These programs provided (1) automatic initiation and termination of ramp control based on real-time traffic information, (2) determination of maximum flow rates for the entrance ramps in real-time freeway operations, (3) ramp metering operational modes based on freeway merging conditions (fixed rate or gap acceptance metering), and (4) extensive analysis programs for study and evaluation of the total system operations (1). The minicomputer, which was installed in 1971, became the primary ramp controller, and the Model 1800 digital computer and the eight-ramp analog controllers now serve as backup central control systems.

This report provides an opportunity to evaluate the minicomputer operations in the specific data acquisition and process control application of freeway ramp control. The report also reviews procedures used during the specification development, system testing, and evaluation periods. In addition, the methods used in establishing the freeway ramp control logic in a given small digital computer are included. This report demonstrates the feasibility of using a small digital computer for freeway ramp control.

SYSTEM DEVELOPMENT

In the earliest development stages for the minicomputer system, the capabilities and constraints that were to be required of the system were established. The four major functional requirements of the minicomputer system were: (1) monitor and control of the present eight entrance ramps without extensive modifications of present equipment, (2) expandability to include the data acquisition and control components for twenty entrance ramps (3) stand-alone operational system, and (4) cost-effective in design and operation. These along with the knowledge gained in developing and implementing the freeway ramp control system in the Model 1800 digital computer, were used in conducting a survey in 1969 on the then available small digital computers. In conducting the survey, particular emphasis was directed towards the organization of the memory, central processing unit (CPU), input-output (I/O), and interrupt structures of the small computers as might be applicable to freeway ramp control. Detailed information was accumulated on each machine and arranged in accordance with the guidelines as documented in Appendix A. The results of the survey indicated that several minicomputers could be used if certain limitations were placed on the systems. For example, some machines contained an ideal interrupt structure but undesirable I/O or CPU functions. It was not known at that time exactly how many modifications would be made by the minicomputer manufacturers in order to meet the requirements of the application. Of the manufacturers that were contacted, several indicated that some additions and modifications could readily be accomplished without extensive redesign of their equipment. Other manufacturers gave

little information to the facility of equipment modification. Therefore, armed with the requirements of the application and the present minicomputer offerings, specifications were developed. The minicomputer described in the specifications was the machine that would best fit the application and did not necessarily describe a particular marketed machine. It was understood that by approaching the specifications in this manner, a system exactly matching the specifications might not be received. This approach would enable the minicomputer manufacturers to participate in the bid presentations in the most comprehensive manner by bidding alternatives, and not to be restraicted to responses in the familiar "or equivalent device" manner. Appendix B contains highlights of the minicomputer selection from those systems bid and the system performance acceptance tests are explained in the following sections.

Procurement and Testing

The specifications for the minicomputer contained an adequate description of the minimum requirements that were necessary for the ramp control computing system and a manufacturer could satisfy the overall objectives of the specifications while deviating from specific requirements. Each manufacturer was to identify any such deviations and show that the deviations did not adversely affect the achievement of the overall objectives as expressed in the specifications. Each manufacturer was also requested to give further information about its proposed computing system. This information would be used in the event that all bids would not completely satisfy the specification requirements, but a recommendation for the acceptance of a system was requested.

After receipt of the bids, a detailed comparison of each system against the specifications was made. Table 1 lists the basic information used in the analysis. Each item of the specifications, an explanation of that item as bid by each manufacturer and an indication as to its compliance with the specifications were included in the analysis. The conclusion drawn from this analysis was that no system completely satisfied the specifications. The results of this analysis and the additional information from the manufacturer were used in a rating evaluation. This rating considered five factors: (1) software, (2) hardware, (3) maintenance, (4) delivery date, and (5) company rating. Each factor was assigned a relative value based on the specification requirements and the extent to which a bid satisfied those requirements. The sum of the five ratings was charted against the bid prices for each system (Figure 1). Several conculsions were drawn from the rating analysis.

First, either the minimum requirements for the minicomputer ramp control system were too restrictive, or the manufacturers were not prepared to provide the total computing system. As indicated in Figure 1, only one of seven systems bid exceeded the minimum requirements for the computing system. The second conclusion is that while nationally advertised prices for these minicomputers in basic configurations were well under $20,000 for six of seven systems bid, the bid quotes were all substantially greater than these prices. The reason for the increased prices is attributable to special I/O devices, packaging of the total system, installation, and other non-standard items. Also, the economic recession experienced in 1969 by the computer industry may have influenced the bid quotes.

TABLE 1

BID RESPONSE CHECK LIST AGAINST SPECIFICATION

Specifications	Explanation	Compliance With Specifications
Central Memory		
Cycle Time		
Addressing		
Instruction Set		
Hardware M/D		
Interrupt Control		
Timers		
TTY		
Console		
Mainframe Cabinet		
I/O Interface & Control		
Software		
Operating Environment System		
Performance & Penalty Test		
Hardware & Software Support		
Installation		
Maintenance & Cost		
Warranty		
Training		
Shipment		

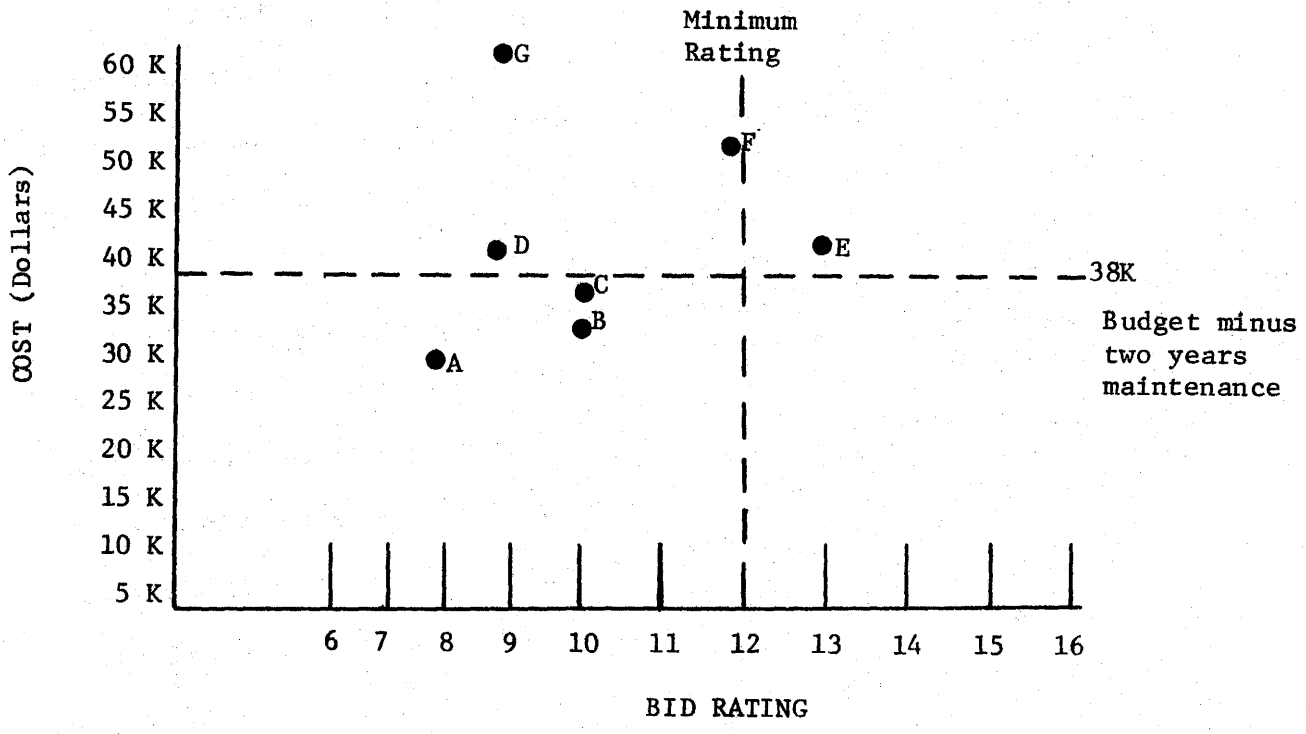

Figure 1. Bid rating vs. cost.

System G in Figure 1 was the only bid received from a traffic control equipment manufacturer even though several received bid solicitations. A conclusion to be drawn is that suppliers of traditional traffic control equipment were unable to supply a traffic control device in the form of a small digital computer. Another way to state this is that central control devices in the form of a digital computer may not be secured from traditional traffic equipment manufacturers on a competitive price basis.

Other conclusions drawn from the analysis of the bids were: some small digital computers companies were anxious to venture into a new application area; some bidders did not understand what was required for the application; some computer manufacturers did not want to modify existing equipments; and the ramp control system presented special requirements not common to other process control applications.

After the analysis of the bids, the ratings and costs as presented in Figure 1, there were two courses of action available; revise the specifications to a particular machine and resolicit new bid proposals, or accept one of the bids. It was decided that one of the proposals would be accepted after additional analysis because (1) the basic requirements for the data acquisition and process control application would not change if new bids were solicited, (2) the interface requirements would not change, (3) the probability of no significant change in the basic computing system to be bid was high, and (4) the time frame for project completion was critical. Therefore, the bid systems were reanalyzed from the standpoint of the least difficult to implement. Every system could have been utilized if (1) modification to the existing

equipments were made or (2) different approaches in the control programs were used. Each system was rated based on the following criteria; (1) time spent in learning software, (2) difficulty in control programs changes, (3) difficulty in hardware programming, (4) interrupt control techniques, and (5) the I/O device operations. These adaptability ratings were totalled and compared with the bid prices for each system as shown in Figure 2. In further analysis of these systems, the following criteria were used: (1) rule out those systems which had hardware exceptions that were detrimental to the success of the system, (2) rule out those systems which had taken exception to testing procedures, and (3) rate the remaining systems on ease of use and expandability. This analysis resulted in a recommendation for accepting System C. (Note: In preparation for this report, a review of the evaluation procedures indicated that System C would still be the recommendation, based on the project requirements and systems bid.) The testing of the digital computing system began after the installation in the Control Center.

The first attempt at conducting the acceptance testing of the delivered Model DM-16 minicomputer from Datamate Computer Systems, Incorporated began in May 1971, and ceased shortly thereafter. The basic acceptance test criterion was for the total system to operate for a continuous thirty-day period without any malfunction. During the checkout period, a malfunction in the input modules was discovered, and the test period was suspended. These input malfunctions were not corrected until September 1971, when redesigned modules were installed. With the exception of this recurring malfunction, for which the manufacturer was penalized for the maximum thirty-day period, the computing system operated

TABLE 2

ADAPTABILITY RATING vs. COST

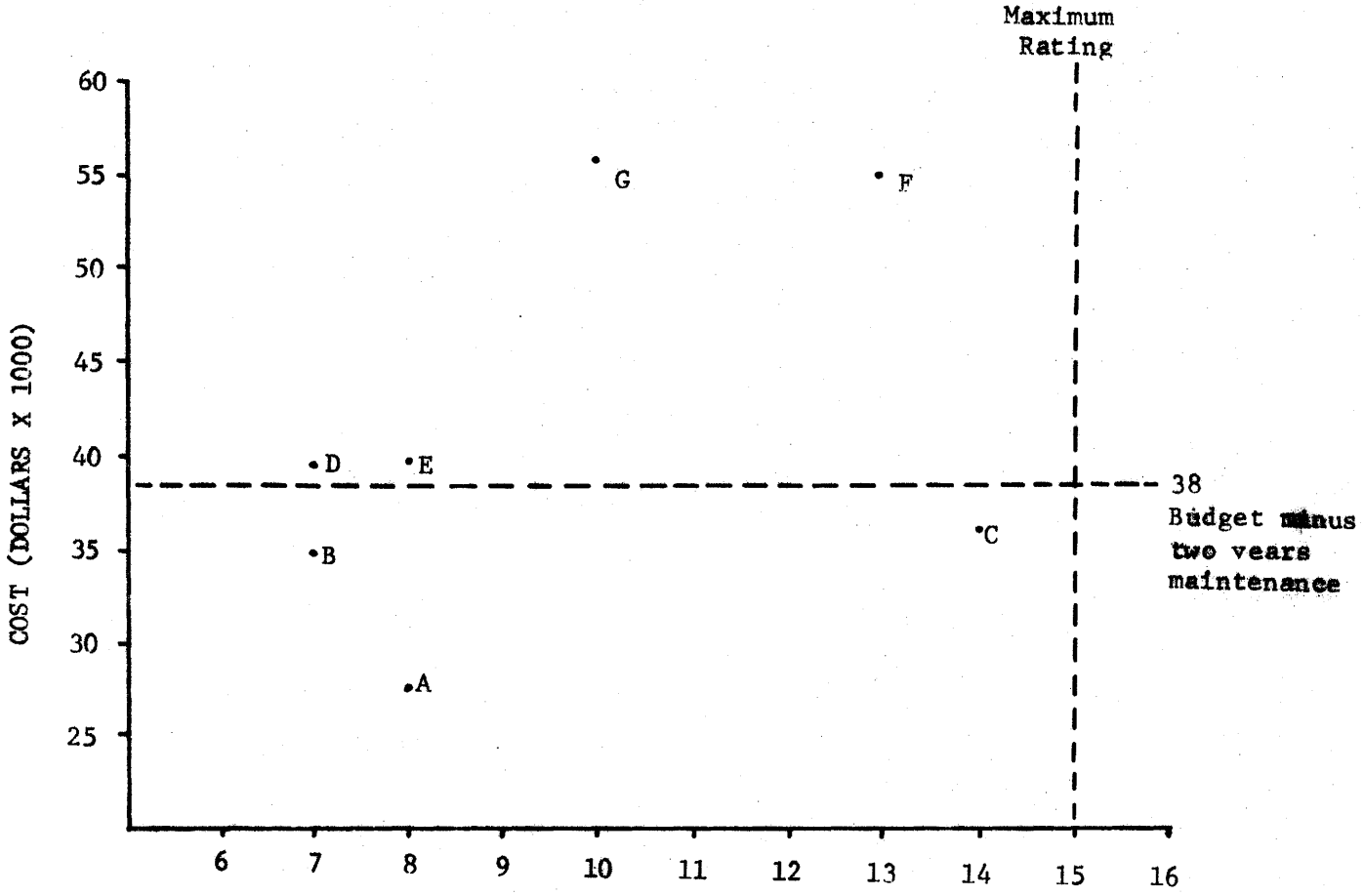

TABLE 3

ACCEPTANCE TEST AREAS

Component	Test Method
Memory	Programs which conducted repetitive read/write to all of core memory
Central Processing Unit	Program which verified the proper results after each instruction had been executed
Interrupt Structure	Programs which verified the proper status of the mask/unmask interrupt operations
Input/Output Structure	Programs which verified the proper operations of all I/O devices of the delivered system
Interval Timers	Programs which operated the two interval timers at all frequencies and checked accuracies
Power Fail/Auto Restart	Programs which verified the operations of the power fail/auto restart feature of the system

as expected. The specific hardware items tested and the methods used in conducting the acceptance test are listed in Table 3. The acceptance testing was accomplished in a modular fashion. Different segments of the computing system hardware were tested with programs specifically written to test that particular series of components. All components of the computing system were successfully tested after the redesigned input modules were installed in September 1971. The time interval between May 1971, and September 1971, was spent in developing application programs for freeway ramp control and itemizing changes for future specifications. Chapter IV discusses the level of effort in the development of application and operating system programs.

Specification Changes

Whenever equipment specifications are developed for the first time, it is difficult to properly assess: (1) what actually should be present in the specifications, and (2) the degree of importance placed on those functional subparts used in arriving at an operational system. This was the case in developing the specifications for the minicomputer system used for freeway ramp control. The following suggestions for changes and additions to the specifications are based on the experience gained from the startup and operating difficulties and reflect the appropriate corrective measures taken within the Datamate DM-16. These suggestions are also based on the assumption that the specifications will be directed towards achieving the same objectives as outlined earlier.

The requirements for any additions to specifications for a real-time data acquisition and process control application should basically enhance the operation

and reliability of the system. The hardware items that would present a more reliable operating system are included in Appendix C and basically contain: (1) a storage protect feature for the memory, (2) an interval timing device driven from the frequency of the AC power source, and (3) an interrupt structure with a reliable power fail/auto restart feature. The storage protect feature would enable protection for critical programs and data areas. The interval timing devices should be driven directly from the AC power source or provide an equivalent long term accuracy so that long time periods (days) will be accurate. Long time extended time period accuracies from timing devices driven by vibrating crystals may not yield acceptable periods. Finally, an interrupt structure should be designed so that the power failure/automatic restart feature (PF/AR) is unmaskable and always enabled. It was found that this PF/AR operation could bring the computing system to a halt if the AC power source rapidly fluctuated. These three items are the most critical hardware features that should be added to the specifications for increased system reliability.

Additions to the specifications that would enhance the operating capabilities of the computing system fall into two categories. The first area would be a prebidder conference in which questions concerning the proposed system could be answered. In new application areas where previously unused equipments are proposed, this conference should be held to insure that the original intent of the application and specification is more fully understood. The second area includes those items that would decrease the time spent during program development, debugging, and implementation. These items could be leased for a specific period of time and could include a card read/punch, line printer, and high speed paper

tape devices. In Appendix C, these additions to the specifications are the minimum items that would increase the operating capability and reliability of the computing system.

Summary

The effort expended in trying to specify and procure a digital minicomputer suitable for freeway ramp control resulted in a decision being made between (1) directing the requirements of the ramp control application to that of a particular minicomputer and (2) accepting a computing system that most closely satisfied the requirements of the application. Survey results indicated that several minicomputer systems could be configured for a freeway ramp controller. Specifications were developed around a computer system that would best satisfy the requirements. The bidders quotations received indicated that several of the manufacturers limited participation in their presentations to standard off-the-shelf systems. Analysis of the quotations suggested the acceptance of a minicomputer system that could be configured as the central freeway ramp controller within the original intent of the specifications. Acceptance of the delivered minicomputer system was delayed four months while the manufacturer completed the redesign and implementation of input modules which had met specifications but would not function properly. During the testing and evaluation periods, those functioning subcomponents which adversely affected the performance of the ramp control system became the criteria for the changes and additions to the specifications.

The knowledge and experience gained in the procurement and implementation of the Datamate Model DM-16 minicomputer should provide additional guidelines and information to observe for future real-time data acquisition and process control systems.

OPERATION EVALUATION

During the system acceptance testing period, the primary objective was the verification that the complete computing system functioned as specified. Two principal areas were investigated during the evaluation of the DM-16 minicomputer as a freeway ramp controller. The first was concerned with the operation of the data acquisition and ramp control programs within the DM-16 minicomputer. Without a satisfactory level of confidence in the operation of these programs, it was impossible to enable the DM-16 minicomputer to control the freeway entrance ramps. These programs, and their associated subprograms, required the proper functioning of both the operating system software and the hardware I/O modules. Therefore, a series of data comparison tests were conducted in which freeway data measured by the model 1800 and the DM-16 minicomputer in real-time, taken from shared sensor inputs, were collected. It was through the analysis of the results of these tests that the integrity of the programming logic, sensor input allocations, and freeway data measurements were documented. The test results in this first investigated area are included in the following subsections.

The second investigated area was concerned with the actual operating reliability of the DM-16 minicomputer. The examination into the operation of the DM-16 control system included hardware, software, and any other factors external to the DM-16 minicomputer which influenced the operation of the control system. Basic tests of measurement methods are included in the discussions concerning these items.

Data Integrity

A measurement standard was established to evaluate the accuracy of data measurements by the DM-16 minicomputer. Two assumptions were used to arrive at a method for the evaluation criteria. First, an acceptable accuracy had been obtained during freeway ramp control operation with the Model 1800. Second, the DM-16 would monitor the same sensor inputs as the 1800. This meant that both computers would be capable of responding to the same sensor indications at the same time. If the sensor measurements from both computers resulted in equal results, then the DM-16 would have to be as accurate as the 1800. Therefore, a series of comparison tests were devised and implemented in the two computers.

Micro-Data Test - Data from a 100-vehicle sample was collected over a chosen sensor. As each vehicle passed over the sensor, both computers measured the length of time to the nearest millisecond that the sensor was activated by the vehicle. Also, the time headways between vehicles were measured for total elapsed time comparisons. By comparing the passage times of occupancies as measured by each computer, it was possible to evaluate the accuracy of the DM-16 freeway speed measurements by assuming an effective detection zone or an average vehicle length of eighteen feet. Table 4 contains a partial listing of a test conducted on the Griggs DA sensor. There is a one to three millisecond difference in the travel times. When these times are converted to the nearest mile per hour speeds, there is essentially no difference. There is a larger timing error in the vehicle headways as measured by the two computers, but the errors are of little consequence. Table 5 contains another comparison test conducted at the Woodridge DA sensor. This partial sample was selected to demonstrate the timing measurements over a

TABLE 4

DATA COMPARISON - GRIGGS DA SENSOR

	DM-16		1800		Speed (MPH)	
Vehicle	Travel Time	Headway	Travel Time	Headway	DM-16	1800
1	0.292	1.392	0.292	1.393	42	42
2	0.288	3.710	0.289	3.714	42	42
3	0.274	7.386	0.273	7.390	44	44
4	0.256	1.340	0.258	1.344	47	47
5	0.254	4.388	0.253	4.389	47	48
6	0.292	4.690	0.293	4.694	41	41
7	0.264	5.964	0.264	5.971	46	46
8	0.300	2.600	0.299	2.601	40	40
9	0.288	6.092	0.289	6.097	42	42
10	0.280	5.970	0.281	5.975	43	43

TABLE 5

DATA COMPARISON - WOODRIDGE DA SENSOR

	DM-16		1800		Speed (MPH)	
Vehicle	Travel Time	Headway	Travel Time	Headway	DM-16	1800
1	0.206	1.994	0.206	1.995	59	59
2	0.202	7.300	0.199	7.306	60	61
3	0.198	1.566	0.205	1.568	61	59
4	0.206	6.148	0.205	6.152	59	59
5	0.809	3.203	0.808	3.204	15	15
6	0.316	6.658	0.317	6.664	38	38
7	0.350	7.568	0.350	7.574	34	34
8	0.284	2.042	0.284	2.043	42	42
9	0.216	2.226	0.217	2.228	56	56
10	0.264	3.844	0.264	3.847	46	46
11	0.196	5.938	0.196	5.944	62	62
12	0.208	1.292	0.207	1.292	58	58
13	0.184	5.020	0.185	5.024	66	66
14	0.260	1.604	0.261	1.606	47	47
15	0.238	4.798	0.239	4.800	51	51
16	0.238	1.972	0.239	1.974	51	51
17	0.230	7.434	0.230	7.434	53	53
18	0.218	3.991	0.219	3.994	55	55
19	0.208	1.266	0.208	1.267	58	58
20	0.212	2.602	0.212	2.604	57	57

larger speed range. Vehicle 5 was a large, slow truck which had formed a small queue behind it. This sample illustrates that the speed of a vehicle does not affect the accuracy of the measurements by the DM-16. The micro-data measurement comparison tests proved that the DM-16 minicomputer was time responsive.

Macro-Data Test - Data were collected over longer time periods from the freeway ramp control system. Flowrate data were collected by both computers for comparison studies. During one sample ten-day test period, the peak one-hour and two-hour flowrates were collected and compared for each freeway and ramp location. Tables 6 and 7 contain the average absolute difference between daily flowrates. Table 7 indicates the average two-hour flowrate over 21 detection locations as calculated by each computer. The averages do not greatly differ, and the average absolute difference is only slightly greater. Considering the total number of vehicles over the two-hour period and the total average absolute differences, the average difference in vehicle counts was between two to three vehicles for every 1000 vehicles counted. This difference in flowrates has been determined to represent a non-significant measuring error for daily ramp control operations in the DM-16 minicomputer. The analysis of the micro and macro data measurements indicated that the DM-16 minicomputer did present acceptable data measurement accuracies when both software and hardware functioned properly.

Operating Reliability

In establishing the integrity of the measured freeway data, the major emphasis was directed towards verifying the accuracies of the volume, speed, and occupancy calculations. The ability to retain this accuracy required

TABLE 6

ONE-HOUR VOLUMES - TEN-DAY SAMPLE

Location		DM-16 Avg.	1 Hr. 1800 Avg.	DM-16 S.D.	1800 S.D.	Avg. Abs. Difference
Frwy.	225	3907	3902	258	255	5
	Wood	4438	4432	214	213	5
	Griggs	4681	4684	202	199	8
	Tele	5006	5004	240	242	3
	Dum	4702	4705	181	181	12
	Cul	4887	4898	152	154	17
Entrance	225	653	651	48	47	1
	35	502	503	73	74	1
	Wood	389	389	80	80	0
	Moss	273	273	29	29	0
	Griggs	235	240	60	61	5
	Way	243	244	14	15	0
	Tele	236	239	23	23	2
	Dum	390	392	56	55	2
Exit	35	437	438	81	81	1
	Wood	174	175	27	28	1
	Moss	66	66	14	14	0
	Way	349	350	36	36	1
	Tele	154	159	43	44	5
	Lom	113	116	12	12	3
	Dum	397	398	55	56	1

TABLE 7

TWO-HOUR VOLUMES - TEN-DAY SAMPLE

Location		DM-16 Avg.	1800 Avg.	2 Hr. DM-16 S.D.	1800 S.D.	Avg. Abs. Difference
Frwy.	225	7807	7809	329	329	4
	Wood	9136	9135	262	262	4
	Griggs	9322	9332	220	220	14
	Tele	10038	10044	268	268	7
	Dum	9237	9232	229	229	29
	Cul	9468	9482	203	203	25
Entrance	225	1591	1591	114	115	1
	35	1170	1168	65	66	3
	Wood	716	717	124	125	1
	Moss	456	456	39	39	0
	Griggs	538	548	112	115	9
	Way	431	432	95	94	2
	Tele	440	444	43	44	3
	Dum	656	661	79	77	4
Exit	35	972	974	161	162	2
	Wood	452	453	48	49	2
	Moss	153	153	17	16	0
	Way	809	810	28	28	2
	Tele	327	336	70	72	8
	Lom	270	274	11	12	4
	Dum	929	931	156	156	2

reliability in the total operations of the DM-16 minicomputer. Therefore, daily monitoring of the freeway ramp control operations was conducted. Whenever a deficiency was discovered which affected the ability of the DM-16 computing system to reliably respond to the ramp control operations, adjustments were made, thereby decreasing the effects of these deficiencies and increasing the reliability of the computing system. In those areas where adjustments were not possible, the deficient items became the criteria for the specification changes or additions. Adjustments were required in both the DM-16 minicomputer and the freeway data input and control output interfaces.

System Timing - One of the first deficiencies encountered during the testing period was the accuracy of the interval timing devices within the Model DM-16 minicomputer. The interval timers are driven from a 10.000 megacycle crystal which is the basic timing element for the entire computing system. These timers are used to schedule program executions which, in turn, keep up with long-time periods (seconds, minutes, hours, etc.). Before the system was manufactured, the Datamate Company indicated that long-time periods (as provided by use of the DM-16 interval timers) would not be as accurate as timers driven from a 60 cps AC line frequency.

Testing revealed that the timing devices employed within the DM-16 gained 2.8 ± 0.1 seconds per hour. Although this did not represent a serious problem to the overall ramp control operations, it did make comparison of freeway data difficult. The Datamate Company indicated that changing the crystal might prohibit the computing system from operating correctly. Therefore, corrective software was implemented which shortened the first minute of each hour by 2.8 seconds. This arrangement enabled acceptable flowrate data to be collected by the DM-16.

This timing error and corrective programming software accounted for part of the errors in both the micro and macro data comparison tests. Present plans include the addition of a digital clock external to the DM-16 which will provide accurate time of day readings even under AC power failure conditions.

Output Modules - Due to the requirement that existing control interfacing relays would have to be retained, the DM-16 output devices had to be rated to switch 48 volts DC through a 2500 ohm control relay coil. Datamate Computer Systems chose to use a circuit module that contained a reed relay. During several months of ramp control operation, three of these relay modules had failed. Tests indicated that the coils were not damaged, but the contacts had fused together. Analysis of this situation resulted in a modification to the control interfacing relay coils that were external to the DM-16 minicomputer. Even though the problem did not exist in the DM-16 design or operations, operational difficulties arose due to this type of external influence.

(Note: The DM-16 minicomputer system was delivered with two output control devices of 16 bits each. The present control method employs two control bits per ramp controlled. A total of sixteen entrance ramps can be controlled without hardware expansion to the existing system.)

Input Modules - After the input module modifications and changes, the daily operations of these modules remained constant. The exception to this type of reliable service occurred during several unusually bad electrical storms. In two cases, lightning entered the Control Center building and induced large voltages into the DM-16 input modules. This type of action caused malfunctions in the input modules which resulted in faulty freeway data. No direct corrective action

can be taken to insure against direct lightning strikes. An operational procedure was implemented which has decreased the possibility of input module damage. At the entry point of the sensor input data into the Computer Room, a removable patchboard panel was installed. The incoming sensor indications are split at this patchboard and connected to the DM-16 and IBM 1800 computers, respectively. Whenever severe electrical storms in the vicinity of the Control Center are first noticed, the patchboard is removed. This disconnects all lean-in wiring to both computers. If the electrical storm happens to occur during the control period, the ramp control operations are switched to the backup analog controllers. Since implementing this procedure, no input device malfunction has occurred.

Power Supply - In a process control environment, it is important that the computing system monitor the primary AC power source. This function normally is completed with circuitry within the main power supply of the computing system. Without AC power, the DM-16 would not function unless backup batteries were provided. It was determined that ramp control operations would cease when AC power interruptions were experienced. The specifications requested automatic power failure and restart functions. These functions were tested in the DM-16 minicomputer without incident and accepted. Four months after beginning the ramp control operations, a malfunction within the power supply developed. An AC voltage 'spike' initiated the automatic failure function which began an orderly shutdown of the CPU and core memory operations. The manufacturer exchanged power supplies and this malfunction has been eliminated.

Another similar malfunction occurs when the AC power rapidly fluctuates. Whenever a series of AC power surges through the fuse protection circuits within

the power supply, the element in the fuse does not dissipate the generated heat fast enough. This causes the fuse to 'blow' which inhibits the DM-16 from operating. The DM-16 is performing the hardware functions as it should, but the AC power is not supposed to experience this phenomenon. The corrective plan is to place a time-delay resumption of AC power for a 15-30 second period after the first power failure interruption.

Summary

The comparative tests conducted on freeway traffic data indicated that the Datamate Model DM-16 minicomputer was as accurate as the IBM 1800 control computer. Individual vehicle speeds were found to be within ± 1 mile per hour while hourly freeway flowrate data differed by 2 to 3 vehicles per thousand. These differences had no effect on the performance of the freeway ramp control system. Daily monitoring of the ramp control operations indicated several deficiencies that affected the operational reliability of the system. Adjustments were made to: (1) the system timing programs for more accurate long-term measurements, (2) the interfacing output control relays which affected the life expectancy of the output devices in the Datamate DM-16, and (3) the operating procedures during the high-noise environment of a nearby electrical storm. The operational reliability of the system within the DM-16 remains high, while maintaining the accuracy of freeway data measurements.

SYSTEM SOFTWARE

The programs that enabled the DM-16 minicomputer to function as a central freeway ramp controller followed three stages of development. First, those programs needed to maintain the computing system hardware were developed. Next, the logic for freeway ramp control, previously developed in the 1800 was translated and implemented for utilization in the DM-16. The last stage involved system support programs which were used for gathering information about the DM-16 operations. A brief description of the implementation procedures and the required level of effort are included in the following subsections.

Operating System

The major portion of the software for any operating system is devoted to recognizing interrupts, scheduling program executions, and handling the I/O requests. The DM-16 minicomputer provided an interrupt structure which was arranged into priorities as established by the freeway ramp control philosophy. The architecture of the DM-16 enabled the initiation of hardware interrupt using a software instruction. This feature, combined with the ability to time events through the use of interval timers, enabled the operating system's hardware in the DM-16 to be minimal in size and complexity. The only software required for the computing system's operations are routines used to regulate the control of the ASR-33 teletype - paper tape I/O device. The interrupt hardware conducts and coordinates all program scheduling based on real-time or programmed interrupts. Table 8 lists the arrangement of the system software by priority of program

TABLE 8

DM-16 Freeway Ramp Control Software System

Priority	Level	Program Name	Interrupt	Function	Data
Highest	0	ITC	Real Time Interval Timer	Schedules Level 3,4	Minute of Day; Day of Week; Day of Month; Month of Year
Next Highest	1	DAS	Real Time PI Module 1	Services DA Sensors	Speed, Volume, Occupancy; Travel Time, On-Time
"	2	MIDS	Real Time PI Module 2	Services 8 Mid Sensors	Speed, Volume, Occupancy
"	3	RCON	Programmed 0.1 Second	Services 8 Entrance Ramps	Scans 80 sensors; Sets Volumes, Occupancies; Selects, Measures, Projects Gaps; Sets Overrides; Change Signal Indications
"	4	SUPER	Programmed 60.0 Second	Services Freeway Operations	INPUT - Gathers volumes, speeds, occupancies; TONOF - Initiates/terminates ramp control; MCSAL - Set metering rates based on freeway conditions MONST - Stores ramp conditions for last minute OUTPUT - Log on TTY last freeway conditions
"	5	ANALS	Programmed Control Period	Logs Operations	Print Ramp Operations; Log Freeway Summary
"	6	LOOPE	Programmed from Console	Tunes Speed Traps	Changes Effective Distance of Speed Traps for More Realistic Speeds
Lowest	7	KEYB	Programmed From Console	Inquires from ASR-33 Keyboard	C - Coldstart System I - Change 1 Word of Core O - Print 1 Word of Core M - Print Page of Core D - Print all Volume Measures X - Exit KEYB Routines
Background	-	----	----------	Executes when Nothing Else in System Is Busy	Waits!

execution.

Due to the operating capabilities of the hardware interrupt structure, the following sequence of events do not require software control. A program currently executing with a given priority level will be temporarily halted by an interrupt request with a higher priority level. The program will remain suspended until all higher priority programs have executed, but will resume execution at the point of suspension when all higher priority interrupts are cleared. The interrupt levels are cleared upon program termination. The program's execution will not be halted when an interrupt requests the execution of a lower priority program. The hardware interrupt system will retain the lower priority interrupt request for later servicing. All operations of this type are conducted and coordinated automatically by the hardware structure of the DM-16 minicomputer.

Freeway Ramp Control

The software programs implemented in the DM-16 for the ramp operations used the basic logic previously developed in the 1800. The developed logic consisted of a series of time responsive subprograms which enable the DM-16 minicomputer to assume the role of a centralized freeway ramp controller. The time responsive subprograms, listed in Table 8, are both real-time and program scheduled. Real-time subprograms (levels 1 and 2) execute whenever the sensors are actuated and sensed by the input devices of the DM-16. Priority level 1 (Table 8) enables the approach sensors at each entrance ramp to be monitored. The sensor indications (level 1) establish the basic data for measurements in the gap acceptance metering (level 3). Level 2 subprograms monitor the center lane sensors at various freeway

locations for speed, volume, and occupancy measures. These measurements are utilized by the freeway operations supervisor programs on level 4. The remaining sensors at the freeway and ramp locations are monitored by programmed scheduling on level 3.

The time scheduled programs, established from priority level 0, execute in three time frames on priority levels 3, 4, and 5. The first program set, ramp control, begins execution every 0.1 second. This series of subprograms accomplishes the following functions: (1) scans 80 sensor inputs, (2) updates volume and occupancy measurements, (3) measures, projects, and selects gaps, (4) determines control override functions, and (5) changes ramp signal indications based on the above criteria. Priority level 4 contains the freeway supervisor program set which executes each 60.0 seconds and consists of five subprograms. Freeway measurements are collected each minute and are arranged into meaningful data by the INPUT Routine. Routine TONOF determines the initiation and termination of the ramp control operations at each ramp based on freeway conditions and time of day. The metering and gap acceptance parameters are determined by the freeway conditions in routine MCSAL. The MONST routine calculates and retains the metering and merging operations data at each controlled ramp for post-period analysis. Finally, the OUTPUT routine delineates on the teletype requested freeway conditions of volumes, speeds, and occupancies for consideration and evaluation by the engineer in charge.

The final time scheduled set of subprograms execute on priority level 5 at the close of each control period. The first set of analysis routines generates the flowrate data over freeway and ramp detection locations for the two-hour and

peak-hour periods. The evaluation of these flowrate data defines the effectiveness of the daily ramp control operations.

System Support

The third phase in the software development for the DM-16 ramp control operations included the two lowest priority levels of program execution. Level 6 contained the speed trap adjustment routines which enabled more correct speed measurements to be taken from the sensors on levels 1 and 2. Level 7 contained several routines by which: (1) the total computer operations can be restarted with the proper time clock setting, (2) core memory values can be documented on the teletype, (3) core memory can be changed, and (4) the data printouts of all sensor indications can be obtained over the last five minutes (used as a detector check). These support routines proved invaluable during system startup and testing periods. Presently, these interrogation-type routines provide a means of documenting changes or additions to the system.

Level of Effort

The development of the DM-16 ramp control system software required 5 man-months of effort by the project staff. Table 9 indicates the staff allocation requirements and amount of time spent. At each stage in the system development, four basic steps were followed: (1) planning the work to be accomplished, (2) coding the program instructions, (3) checking the accuracies of the programs in real-time, and (4) documenting the resulting operations. Although each step has been separated for report clarity, many functions overlapped. For instance, during

TABLE 9

STAFF ASSIGNMENTS

Man-Months

Classification	Planning	Coding	Debug	Docum-N
System Programmer	1	2	1/4	1/4
Keypunch Operator		1	*	
Electronic Technician	*		1/4	1/4
TOTAL	1	3	1/2	1/2

the coding of the program instructions, much of the documentation was implemented as comment statement. Figure 2 represents a manpower requirement for each step for the duration of the three stage development cycle.

Planning

Planning occurred at various points in time during the development of the freeway ramp control system. The first preliminary planning occurred during the bid response evaluations. At that time, all computers bid were configured in a simplified freeway ramp control mode. The second planning period occurred before and during the system acceptance testing. The plans included system testing programs (levels 0-3) that could be utilized later when the testing was completed. Final planning was accomplished when the logic for the ramp control program sequence and the later support programs were developed.

Coding

The coding of the program instructions involved the following sequence of events: (1) develop program instructions from logical statements established in planning, (2) keypunch, on paper tape, the source instruction mnemonics in Datamate DM-16 assembly code, (3) list generated object code and punch, on paper tape, the object program (4) load object tape into computer, (5) execute programs and check results (debug), and (6) correct source tape and retrace items 3 through 5 above. Many extra hours of time were spent in the keypunching and program listing sequence due to the slowness of the ASR-33 teletype.

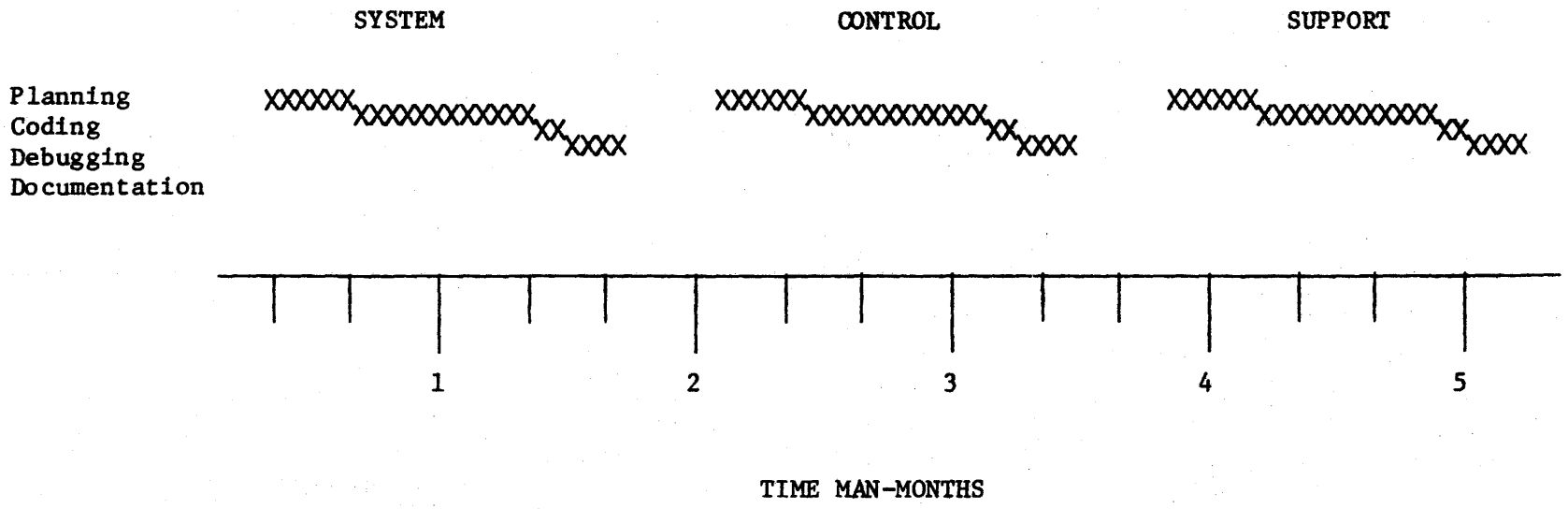

Figure 2. Effort Areas vs. Time

Checkout

The checkout of the programs or routines usually consisted of running the programs in real-time. If the program results were not as anticipated, reasons were found for the different results. If small changes were found to correct the situation, 'patches' were made to the source tape.

Documentation

Documentary efforts included: (1) comment statements in the source instruction program listings, (2) wiring list charts of the input and output devices of the DM-16, (3) page charts of sensor information location and measurements, and (4) organizational lists of program sequencing. The updating of program listings and comprehensive documentation will be accomplished as more control processes (Driver Communications) are added to the DM-16.

Summary

The programs that enabled the Datamate Model DM-16 minicomputer to function as a freeway ramp controller were completed in three basic periods of time. Each stage in the development of the system included program planning, coding, checkout and documentation. The operating system was developed around the hardware interrupt operations of the Datamate DM-16. The eight interrupt levels of the DM-16 minicomputer were assigned a priority of program execution based on the requirements of the freeway ramp control application. The major role in the operating system is scheduling program executions, which are conducted and coordinated by the interrupt hardware.

The second program set was developed from the previous ramp control logic. Real-time freeway data are sensed and calculated by programs executing on priority assigned levels 1 and 2. The ramp control logic is separated into three basic programs. The ramp controller routines execute on priority level 3 each 0.1 second. Every 60.0 seconds, the freeway operations supervisory routines execute on level 4. Freeway data, collected over the last minute, are used to determine the status of the freeway operations, and if necessary, adjustments are made to the metering parameters in the ramp controller routines. After each control period, analysis routines, executing on level 5, document the freeway operations for evaluational consideration.

The final program set includes routines that execute on levels 6 and 7. Speed adjustments are made by the loop tuner programs on level 6. Interrogation routines utilize level 7 for status checks of the minicomputer's operations, as well as providing entries into the real-time ramp control operations. The orderly operations of the hardware of the computer system, combined with the priority assigned logic of the ramp control software, enables the Datamate Model DM-16 minicomputer to control the freeway entrance ramps.

REFERENCES

1. Ritch, Gene P., "Digital Computer Programs for The Ramp Metering System on the Gulf Freeway," Texas Transportation Institute, Research Report 139-12, 1971.

APPENDIX

APPENDIX A

Manufacturer/Model Number

Memory

Memory cycle time (us)

Memory word length (bits)

Minimum memory size (words)

Memory increment size (words)

Maximum memory size (words)

Parity check (std., opt., no)

Memory protect (std., opt., no)

CPU Features

Instruction word length (s)

Number of accumulators (or general purpose registers that can be used as accumulators)

Number of hardware registers (not including index registers)

Number of index registers (indicate whether they are hardware, memory or other techniques)

How many bits for operation code

How many bits for address modes

Number of addressing modes

How many bits for address

In this machine one can directly address _____ words in _____ us and indirectly address _____ words in _____ us

Indirect addressing (multi-level, single-level, no)

Arithmetic Operations

Store time for full word (us)

Add time for full word (us)

Fixed point hardware mult/divide (std., opt., no)

Multiply time - hardware (us)

Divide time - hardware (us)

Multiply time - software (us)

Divide time - software (us)

I/O Capability

Data path width (bits)

Direct memory access (DMA) channel (std., opt., no)

Maximum DMA word transfer rate

Number of external priority interrupt levels provided in basic system

Maximum number of external interrupts

Response time (us) including time to save registers of interrupted program and initiate new program execution

Other Features

Power failure protect (std., opt., no)

Manufacturer/Model Number

Automatic restart after power failure (std., opt., no)

Real-time clock or internal timer (std., opt., no)

Software

Assembler (1 pass, 2 pass, both)

Relocatable assembler (yes, no)

Minimum core size necessary to use this relocatable assembler

Macro assembler capability

Compilers available (specify explicitly e.g., Fortran II, IV, ASA Basic Fortran, etc.)

Conversational compilers (e.g., FOCAL, BASIC, CAL, etc.)

Real-time executive monitor available (yes, no)

Disc operating system available (yes, no)

Basic Mainframe Costs

Basic system price with 4K words including power supplies

Price of ASR-33 Teletype (if not already included in Basic System Price)

Total system price, including ASR-33 Teletype and CPU

Basic system price with 8K words including adequate power supplies, enclosure, control panel

Price of ASR-33 Teletype (if not already included in Basic System Price)

Total system price including ASR-33 Teletype and CPU

Peripherals Available

Magnetic tape available (yes, no)

Approximate price for operational unit (including controller, computer options necessary, etc.)

Mass storage device available (yes, no)

Approximate price of operational unit (including controller, computer operations necessary, etc.)

High speed paper tape reader (yes, no)

Speed (char/sec)

Approximate price of operational unit

High speed paper tape punch (yes, no)

Speed (char/sec)

Approximate price of operational unit

APPENDIX B

Basic Hardware Requirements

Memory - 16K, 16 bits/word, 2's complement, 2 microseconds or less cycle time core

CPU - 4 general purpose registers, hardware multiple/divide

Addressing - absolute, direct, indirect

Priority - Interrupt control of eight program maskable levels with software program interrupt and two unmaskable internal levels

Power Fail/Auto Restart Feature

Two programmable timing devices

ASR-33 - Teletype with paper tape I/O

Console with appropriate switches, controls, and clock with key

Computing System (with exception of freestanding TTY) - enclosed in vertical cabinet with sufficient room for twenty, 16 line terminals

Process I/O - 2-16 bit interrupt modules, and

5-16 bit non-interrupt modules

2-16 bit output devices

All inputs to be isolated

Basic Software Requirements

Basic assembler and FORTRAN

Complete documentation of all delivered hardware and software

Miscellaneous

Performance test period with penalty clauses

Payment in full at successful completion of performance test

List of minimum instruction repiroire

Physical equipment layout diagrams

APPENDIX C

SPECIFICATIONS - ADDITIONS OR CHANGES

Hardware	
Core Memory	Provide a software controllable storage protect feature
Timing Devices	Directly powered from AC line frequency
External Clock	Separate clocking device accurate to nearest minute of day powered by battery source upon AC power failure
Interrupt Architecture	Auto restart interrupt shall be recognizable and unmaskable under all conditions where applicable
Power Supply	Should not blow main fuses on fluctuating AC power failures
Support	
High Speed Paper Tape I/O	Could be leasable for specific period of time to expediate system building
Card Read/Punch	Could be leasable for specific period of time to expediate system building
Printer	Could be leasable for specific period of time to expediate system building
Conference	Pre-bidders meeting held to more fully explain intent of proposal